KU LEUVEN

ARENBERG DOCTORAL SCHOOL
FACULTY OF ENGINEERING SCIENCE

Microsystems encapsulation using nanoporous alumina

Joseph Eid Estafanous Zekry

Supervisors:

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Prof. Jean-Pierre Celis

Dissertation presented in partial fulfillment
of the requirements for the degree of
Doctor in Engineering Science

June 2014

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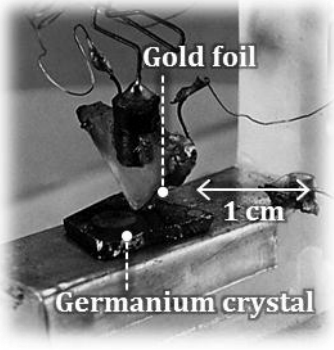
Preface

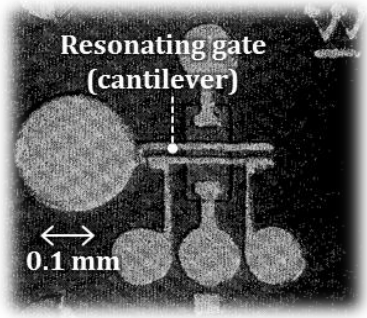
Integrating a microsystem in society

In 1947, fellow researchers John Bardeen and Walter Brattain were working on an interesting new assignment after joining the Solid State Physics research group—founded by William Shockley in 1945—at *Bell Telephone Laboratories* in Murray Hill, New Jersey. Their task was to construct a new signal amplifier using a semiconductor in order to replace the fragile and bulky vacuum tubes used in the *Bell Telephone System* that was pioneered seven decades earlier by Alexander Graham Bell. Knowledge of semiconductors had surged during World War II due to the need for early warning systems (radars) for protection from aircraft attacks. New technologies were developed to produce semiconductor crystals, like germanium, to be used as high frequency signal rectifiers in the new radars.

Bardeen and Brattain used the opportunity of having the new semiconductor crystals in their hands to perform their research which reached a significant milestone just before the Christmas holidays of 1947. On Tuesday, December 23, executives at Bell Labs could hear the amplified signal of Brattain's voice produced by a new electronic device. Ingenious yet simple: Brattain glued a small strip of gold foil around the edge of a triangular plastic wedge. Then he carefully slit the foil using a razor blade at the corner of the wedge. This wedge corner was subsequently pressed against a germanium crystal lying on top of a metal plate. The small (*micro*) slit between the two foil segments allowed Bardeen and Brattain to dramatically alter the germanium conductivity underneath one end of the foil using a small input voltage applied at the other end. Consequently, the input voltage signal was converted into a large (or amplified) current signal using this new *point-contact transistor*.



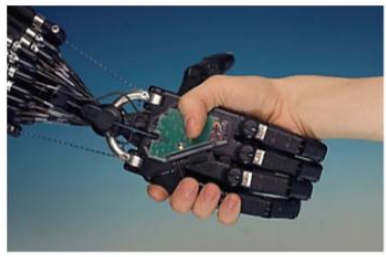
Following the successful demonstration of the first transistor at Bell Labs, the world would witness mounting interest in this new electronic device with rapid development of the theory and technology behind it. Eventually, in 1956, the Nobel Prize in Physics was awarded to Shockley, Bardeen and Brattain for their pioneering work on the transistor effect. The fascinating new field of microelectronics then started attracting many talented engineers and researchers who would enrich it even more with countless innovations. One such engineer, the fresh Ph.D. graduate Harvey Nathanson, joined the Westinghouse Research Labs in Pittsburgh, PA, in 1962 to work on an interesting project together with the skilled laboratory technician Robert Wickstrom. With inspiration from their boss William Newell, they decided to grant the transistor an extra degree of freedom in order to overcome its known instability when used in frequency-selective (filtering) circuits. By 1965, they had already fabricated and tested new transistors with a free-standing (cantilever) gate. They called it a *resonant gate transistor* which was a clever approach at that time to produce circuits with a stable operating frequency defined by the mechanical resonance of the cantilever gate. More importantly, this new transistor became the forerunner of a new generation of microsystems known as micro-electro-mechanical systems (or *MEMS*).



One of the major advancements in the field of microelectronics was more recently recognized by the 2000 Nobel Prize in Physics for Jack Kilby for his pioneering work on the *integrated circuit* (IC). In the late 1950's, while starting his new career at Texas Instruments, Kilby realized how inefficient and expensive it was to pack many different electronic devices into a complex circuit. Therefore he proposed to integrate all transistors, resistors and capacitors of an electronic circuit on the same semiconductor chip. Kilby's ideas were further refined by Robert Noyce who co-founded Intel—where the first microprocessor chip was made in 1971. Merely a decade later, the IBM personal computer was introduced, commencing the age of information technology as we know it today.

Another co-founder of Intel (Gordon Moore) noticed in the 1960's that the number of transistors in an IC has been exponentially increasing with time. This observation—which surprisingly still holds until today—is widely known as Moore's law. This increasing complexity of IC's is a result of the constant reduction of the transistor size and production cost by the microelectronics industry. To grasp the scale of this trend, try comparing an early 1970's

transistor which occupied around 300 μm^2 of the chip area at a cost of ten cents to a modern transistor which occupies only 0.003 μm^2 of the chip area with an associated cost of less than ten millionths of a cent! This technological revolution facilitated the penetration of transistors and other microsystems into almost every aspect of our life. In our modern society, we rely on a continuous flow of information on electronic displays through wired and wireless telecommunication links. Meanwhile, the growing human needs, the limited natural resources and the increasing energy cost are transforming all our buildings, machines, cars, tools, and even cloths into *intelligent things* with the help of complex networks of electronic sensors, displays and control systems.



This seamless integration of transistors, sensors and other microsystems in our society was only possible in the presence of an almost perfect interface between these miniature devices and their surroundings. An *electronic package* facilitates the functionality of each microsystem while protecting its sensitive contents from their "natural predators". Take for example the frequency of rain falling in Belgium—that is around 200 days per year. If the IC's and sensors inside the smartphones in our pockets or purses were not sealed from this continuous flow of water (humidity), the complex network of tiny metal interconnects in every chip would corrode and eventually break in a matter of days. This is just one example from a long list of the hazards that endanger modern microsystems. This list also includes dust, temperature variations, mechanical stresses, shocks, vibrations, light, electromagnetic radiation, and even air in many cases. Because of this diversity of potential risks, the package of a microsystem is becoming rather difficult to miniaturize at the same rate its contents are shrinking. Despite the daily reports of new nano-transistors and nano-sensors, we seem to be continuously relying on the same old electronic package (essentially a millimeter-sized plastic box with metallic contact tips). Only real innovation and profound understanding of the packaging science will allow us to see the day when the size of an electronic package is only a few—instead of a hundred or a thousand—multiples of the size of the small microsystem it encapsulates.

References and photo credits: Bardeen and Brattain, 1949; Nathanson *et al.*, 1965, 1967; Kilby, 1976; Riodan *et al.*, 1999; Thompson and Parthasarathy, 2006; Stephan *et al.*, 2012; www.wikipedia.com; www.shadowrobot.com

"If I have seen further it is by standing on the shoulders of giants."

Isaac Newton (1642–1727)

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Joseph Zekry

Achel, Belgium

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Abstract

Packaging of traditional integrated circuits (IC's) has been reliant for several decades on the techniques of metal bonding and plastic overmolding. However, such conventional packaging techniques are failing to cope with the rapidly shrinking IC dimensions and the growing variety of new microsystems (like micro-electro-mechanical systems, or MEMS) used in modern appliances including biomedical implants and smartphones. In this context rises the need for this research to set a step forward in the direction of package miniaturization, improved reliability and increased functionality of state-of-the-art microsystems.

This thesis deals with the technological challenges as well as with the design and performance aspects of new micropackages created using thin membranes of nanoporous alumina. The new micropackages are intended to encapsulate microsystems—and MEMS in particular—at wafer-level in a controlled environment. Such a micropackage can accommodate one or more microsystems in a planar microcavity of 1 to 10 µm height with lateral dimensions between 0.1 and 1.0 mm. The on-wafer microcavities are formed by etching a sacrificial layer underneath nanoporous alumina membranes of 1 to 3 µm thickness. These membranes feature a large density of cylindrical nanopores with diameters between 10 and 20 nm and height equal to the thickness of the membrane; facilitating the sacrificial layer etching process. A novel wafer-level anodization process performed at a temperature close to 30 °C is developed to produce fully perforated nanoporous alumina membranes within an Al thin film in a single fabrication step. A specially designed photoresist mask is used to define the lateral shapes of the alumina membranes with high precision, while maintaining a low-resistance path for the anodization current across the large area of a 200 mm wafer. A controlled environment inside the microcavities is achieved during a process of depositing an impermeable sealing layer on top of the nanoporous alumina membranes. The resulting micropackages typically feature dielectric (and

optically transparent) caps with a thickness between 4 and 9 μm. The caps are normally anchored around the microcavities using an Al-based sealing ring of 10 to 50 μm width. Empty micropackages of different shapes and configurations as well as encapsulated RF transmission lines and other microsystems (like Ni-based MEMS) have been produced on 200 mm Si wafers. Moreover, micropackages with sufficient robustness to undergo a plastic overmolding process—performed at high pressure of 30 bar and a high temperature of 175 °C—have been designed, fabricated and tested.

Analytical and finite element models have been developed to analyze the thermomechanical and electromagnetic characteristics of the new micropackages and the embedded microsystems. These models provide much insight into the strength, reliability and compatibility of the micropackages with different applications. Furthermore, experimental studies of the hermeticity and reliability of the new micropackages are presented. An extensive hermeticity analysis is carried out based on optical monitoring of the cap deformation under different environmental conditions. This includes short-term (less than 10 days) exposure to helium at 3 bar pressure and long-term (up to 14 months) exposure to air under atmospheric pressure. In this experiment, the significant impact of the sealing ring configuration on the package hermeticity is demonstrated. Moreover, other methods for hermeticity evaluation, including the use of an embedded microresonator or micro-Pirani gauge, are discussed. Additionally, the outcome of a comprehensive set of reliability tests is presented; including the impact of repeated exposure to mechanical shocks and extreme temperatures, in addition to exposure to high humidity levels (at high temperatures). Finally, the compatibility of the new micropackages with radio frequency (RF) microsystems is evaluated. Special Al-based feedthroughs—that can transmit high frequency signals through the package boundaries with minimal added losses—have been designed, implemented and tested.

Samenvatting

Het verpakken van traditionele geïntegreerde schakelingen (IC's) is voor vele decennia afhankelijk geweest van de technieken van metaal verbinden en plastic spuitgieten. Nochtans kunnen dergelijke conventionele technieken niet omgaan met de snel krimpende IC afmetingen en de groeiende verscheidenheid aan nieuwe microsystemen (zoals micro-elektromechanische systemen, of MEMS) die gebruikt worden in moderne apparaten waaronder biomedische implantaten en smartphones. In deze context is de nood aan dit onderzoek ontstaan om een stap verder te zetten in de richting van een verdere verkleining en een verhoogde betrouwbaarheid en functionaliteit voor state-of-the-art microsystemen.

Dit proefschrift behandelt zowel de technologische uitdagingen alsook het ontwerpen en de prestaties van nieuwe microverpakkingen die gemaakt worden met behulp van dunne membranen van nanoporeuze alumina. Deze nieuwe microverpakkingen zijn bedoeld voor het inkapselen van microsystemen—en vooral MEMS—op wafer-niveau in een gecontroleerde omgeving. Zulke microverpakking kan één of meerdere microsystemen inkapselen in een vlakke microcavity met een hoogte van 1 tot 10 µm en een breedte tussen 0,1 en 1,0 mm. De microcavities worden gevormd door het etsen van een dunne laag onder nanoporeuze membranen met een dikte van 1 tot 3 µm. Deze membranen beschikken over een grote dichtheid van cilindrische nanoporiën met diameters tussen 10 en 20 nm en met een hoogte gelijk aan de dikte van het membraan; hetgeen het etsen van de onderliggende laag vergemakkelijkt. Een nieuw uitgevonden anodisatieproces op wafer-niveau dat uitgevoerd wordt bij een temperatuur rond 30 °C is ontwikkeld om doorlatende membranen van nanoporeuze alumina te produceren in een Al-dunne laag doormiddel van één enkele fabricatiestap. Een speciaal ontwikkeld fotoresist-masker wordt gebruikt om de vormen van de nanoporeuze membranen te definiëren met een hoge nauwkeurigheid, en dit met behoud van een pad met een lage weerstand voor de anodisatiestroom over de grote

oppervlakte van een 200 mm wafer. Een gecontroleerde omgeving binnen de microcavities wordt bereikt tijdens het proces van het deponeren van een ondoorlatende afsluitlaag bovenop de nanoporeuze alumina membranen. De resulterende microverpakkingen zijn meestal voorzien van diëlektrische (en optisch transparante) kappen met een dikte tussen 4 en 9 μm. De kappen zijn gewoonlijk verankerd rond de microcavities met behulp van een Al-gebaseerde afsluitring van 10 tot 50 μm breedte. Lege microverpakkingen van verschillende vormen en configuraties alsook ingekapselde RF-transmissielijnen en andere microsystemen (zoals Ni-gebaseerde MEMS) werden geproduceerd op 200 mm Si wafers. Bovendien zijn microverpakkingen ontworpen en geïmplementeerd met voldoende robuustheid om een plastic spuitgietproces—dat uitgevoerd wordt bij een hoge druk van 30 bar en een hoge temperatuur van 175 °C—te ondergaan.

Analytische en “finite element” modellen zijn ontwikkeld om de thermomechanische en elektromagnetische eigenschappen van de nieuwe microverpakkingen en ingebedde microsystemen te analyseren. Deze modellen hebben veel inzicht in de kracht, betrouwbaarheid en compatibiliteit van de microverpakkingen met verschillende toepassingen voortgebracht. Experimenteel onderzoek van de hermeticiteit en de betrouwbaarheid van de nieuwe microverpakkingen is verder gepresenteerd. Een uitgebreide hermeticiteitsanalyse is uitgevoerd op basis van optische metingen van de vervorming van de kap onder verschillende omstandigheden. Dit omvat een korte termijn (minder dan 10 dagen) blootstelling aan helium bij een druk van 3 bar en een lange termijn (tot 14 maanden) blootstelling aan de lucht (1 bar druk). In dit experiment wordt de grote impact van de afsluitringconfiguratie op de hermeticiteit van de verpakking aangetoond. Verder worden andere werkwijzen voor hermeticiteitsanalyse, inclusief het gebruik van ingebedde microresonators of “micro-Pirani gauges”, besproken. Bovendien worden de resultaten van een uitgebreide set van betrouwbaarheidstests gepresenteerd, inclusief de impact van zowel herhaalde blootstellingen aan mechanische schokken en extreme temperaturen alsook aan een combinatie van extreme warmte en vochtigheid. Tot slot wordt de compatibiliteit van de nieuwe microverpakkingen met radio frequentie (RF) microsystemen geëvalueerd. Speciale doorvoeringen gebaseerd op Al—die hoge frequentie signalen door de verpakkingsgrenzen kunnen transporteren met minimaal verlies—zijn ontworpen, geproduceerd en getest.

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"Nothing in life is to be feared, it is only to be understood. Now is the time to understand more, so that we may fear less."

Marie Skłodowska Curie (1867–1934)

Nomenclature

Acronyms

2D	two-dimensional
3D	three-dimensional
AAO	anodic aluminum oxide (or nanoporous alumina)
AC	alternating current
ADI	Analog Devices incorporated
ads	adsorbed
Al	aluminum
AlO_x	aluminum oxide or alumina (any composition)
Ar	argon
a-Si	amorphous silicon
BEOL	back end of line
BGA	ball grid array
C	carbon
C_2H_5OH	ethanol
CMOS	complementary metal-oxide-semiconductor
CMP	chemical mechanical polishing
CPW	coplanar waveguide
CSP	chip-scale package
Cu	copper

CVD	chemical vapor deposition
DC	direct current
DIP	dual in-line package
Fe	iron
FEM	finite element model
Ge	germanium
GmbH	Gesellschaft mit beschränkter Haftung (company with limited liability)
H	hydrogen
H_2O	water
H_2O_2	hydrogen peroxide
HDP	high density plasma
He	helium
HF	hydrofluoric acid
HRSi	high resistivity silicon
IC	integrated circuit
IMOD	interferometric modulator
Inc.	incorporated
IR	infrared
JESD	JEDEC standard of microelectronics
LPCVD	low pressure chemical vapor deposition
LTCC	low temperature cofired ceramics
μc	microcrystalline
MEMS	micro-electro-mechanical system (or structure)
MIL-STD	military standard
MOEMS	micro-opto-electro-mechanical system (or structure)
MSL	microstrip line
N	nitrogen

N_2O	nitrous oxide
NEMS	nano-electro-mechanical system (or structure)
NH_3	ammonia
Ni	nickel
NOEMS	nano-opto-electro-mechanical system (or structure)
O	oxygen
OH	hydroxide
PAA	porous anodic alumina (or nanoporous alumina)
PC	personal computer
PCB	printed circuit board
PECVD	plasma-enhanced chemical vapor deposition
PR	photoresist
PVD	physical vapor deposition
Q	quality
QFP	quad flat package
RF	radio frequency (0.1–100 GHz)
RH	relative humidity
SAM	scanning acoustic microscope
SEM	scanning electron microscope (or micrograph)
Si	silicon
SiC	silicon carbide
SiF_4	silicon tetrafluoride
SiGe	silicon germanium
SiH_4	silane
SiN_z	silicon nitride (any composition)
SiOC	silicon oxycarbide
SiO_y	silicon oxide (any composition)
SIPOS	semi-insulating polycrystalline-silicon

SMA	surface mount assembly
Ti	titanium
TiN	titanium nitride
TiW	titanium tungsten
TL	transmission line
V	vanadium
W	tungsten
WLP	wafer-level package
Zr	zirconium

Symbols

α	inclination angle of a package edge or pillar [degrees]
Γ	strain gradient [m^{-1}]
γ	shear strain [ratio]
γ_{ij}	shear strain in direction *j* on the plane whose normal is in direction *i* [ratio]
Δf	change in frequency or oscillation bandwidth [Hz]
ΔP	change in pressure [Pa]
Δt	change in time (duration of a test) [s]
Δy_c	change in center deflection of a cap or plate [m]
δ_h	horizontal displacement [m]
δ_v	vertical displacement [m]
ϵ	activation energy of a chemical reaction divided by the gas constant [K^{-1}]
ε	normal strain [ratio]
ε_d	dielectric permittivity [F/m]
ε_{ii}	normal strain in direction *i* [Pa]

ν	Poisson's ratio
π	mathematical constant of the circle circumference to diameter ratio (~3.1416)
ρ	mass density [kg/m^3]
σ	normal stress [Pa]
σ_{cr}	critical stress of buckling in a plate [Pa]
σ_{ii}	normal stress in direction *i* [Pa]
$\sigma_{\max}$	maximum normal stress in a structure [Pa]
σ_{u}	ultimate stress of yield or fracture of an isotropic material [Pa]
τ	shear stress [Pa]
τ_{ij}	shear stress in direction *j* on the plane whose normal is in direction *i* [Pa]
Φ	electric potential or voltage [V]
Ω	ohm (unit of electrical resistance) [V/A]
A_{a}	cross-sectional area of the alumina template in a porous membrane [m^2]
A_{p}	cross-sectional area of the pores in a porous membrane [m^2]
A_{t}	total cross-sectional area of a porous membrane [m^2]
a	proportionality constant [different units]
b	proportionality constant [different units]
C	capacitance [F]
C_{b}	buried feedthrough capacitance [F]
CTE	coefficient of thermal expansion [K^{-1}]
d	diameter [m]
d_{C}	cavity diameter [m]
d_{P}	pillar diameter [m]
E	Young's modulus [Pa]

$\hat{E}$	normalized Young's modulus [ratio]
E_{a}	Young's modulus of isotropic (impermeable) alumina [Pa]
E_{ii}	Young's modulus in direction *i* [Pa]
E_{p}	Young's modulus of a pore or void [Pa]
E_{s}	Young's modulus of a sealing layer [Pa]
ER	etch rate of a surface [m/s]
F	general function [different units]
f	frequency [Hz]
f_0	natural vibration frequency [Hz]
G	shear modulus [Pa]
G_{E}	electrical conductance [S]
G_{Emax}	maximum electrical conductance of a resonating circuit [S]
G_{ij}	shear modulus in direction *j* on the plane whose normal is in direction *i* [Pa]
g	standard gravity acceleration (~9.8 m/s^2)
h_{C}	cavity height [m]
I	electric current [A]
J	electric current density [A/m^2]
k	spring constant [N/m]
k_0	proportionality constant [different units]
L	inductance [H]
L_{b}	buried feedthrough inductance [H]
L_{s}	standard leak rate of a package [Pa.m^3/s or mbar.l/s]
l	length [m]
l_{a}	longer edge length of a rectangle [m]
l_{b}	shorter edge length of a rectangle [m]
l_{bf}	buried feedthrough length [m]
l_{c}	cantilever length [m]

l_{ib}	indicator beam length [m]
l_{S}	edge length of a square[m]
l_{sb}	slope beam length [m]
l_{tb}	test beam length [m]
M	ionizing agent in a chemical reaction (fluid)
M_{A}	molar mass of dry air (~28.7 g/mol)
M_{LG}	molar mass of a leaking gas [kg/mol]
m	mass [kg]
P	pressure or distributed load [Pa]
P_0	atmospheric pressure (~101.3 kPa)
P_1	partial differential pressure of a gas in a leak test [Pa]
P_{r}	reference pressure [Pa]
P_{v}	vapor pressure [Pa]
pH	decimal logarithm of the reciprocal of hydrogen ion activity in a solution (concentration)
Q	quality factor [ratio]
R	resistance [Ω]
R_{b}	buried feedthrough resistance [Ω]
r	one of the polar coordinates (radial distance) [m]
S_{ij}	scattering parameter of an electrical network (ratio of the reflected signal at port *i* to the incident signal at port *j*)
T	temperature [K]
t	thickness [m]
t_{a}	alumina layer thickness [m]
t_{C}	cap thickness [m]
t_{d}	dielectric thickness [m]
t_{s}	sealing layer thickness [m]
V	volume [m^3]

V_a	volume of the alumina template in a porous membrane [m^3]
V_p	volume of the pores in a porous membrane [m^3]
V_t	total volume of a porous membrane [m^3]
w	width [m]
w_A	aluminum extension width above a microcavity [m]
w_B	borderline width [m]
w_b	buried feedthrough width [m]
w_C	cap width [m]
w_E	extension width [m]
w_{ib}	indicator beam width [m]
w_S	sealing ring width [m]
x	general independent variable [different units]
y	general dependent variable [different units]
$y(r)$	radial profile of the deflection of a cap or plate [m]
y_c	center deflection of a cap or plate [m]

Chapter 1 Introduction

In this chapter the basics of electronic packaging and vacuum encapsulation of microsystems are first discussed in order to establish the context and the challenges that motivated this research. Further on, we zoom into the techniques of thin film encapsulation of microsystems with emphasis on the emerging use of nanoporous alumina in this field. The performance metrics of thin film encapsulation are then highlighted. Finally, the main objectives and the structure of this thesis are outlined.

1.1 Basics of electronic packaging

Integrated circuits (IC's) are fabricated in a batch processing fashion where consecutive treatments—like film deposition, photolithography, selective etching, ion implantation and annealing—are applied to silicon wafers of less than 1 mm thickness and up to 300 mm in diameter. An IC chip is only a small part of the wafer, typically 1 to 20 mm^2 in area. In order to effectively embed such a small chip in a larger system or machine, a proper package must be used to provide two vital functions: connection and protection (Gilleo, 2005). The traditional first-level (1-level) dual in-line packaging process shown in Fig. 1.1 illustrates how these two functions are commonly implemented. Connection is carried out by a metal lead frame and thin bonded wires connecting it to the chip, while protection is realized by molding a heated epoxy (plastic) compound around the IC under high pressure (Tummala, 2001).

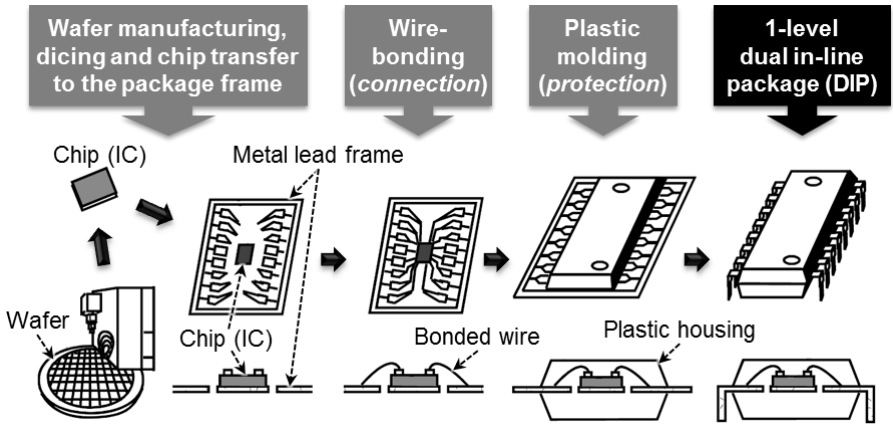


Fig. 1.1 Schematic illustrations of the main steps of the traditional dual in-line 1-level IC packaging process (adapted from: Tummala, 2001).

In applications where the use of a conventional plastic package compromises the performance or the reliability of the system, other (more expensive) materials can be used as a protective housing. For example, the use of a low temperature cofired ceramic (LTCC) as a packaging material is common in high frequency telecommunication systems; given the low dielectric loss of this material and its relative flexibility in terms of processing and integration with other materials (Imanaka, 2006). The use of high-conductivity metals in combination with such ceramic packages is further useful in delivering high frequency signals without large losses and in improving heat dissipation (See Fig. 1.2).

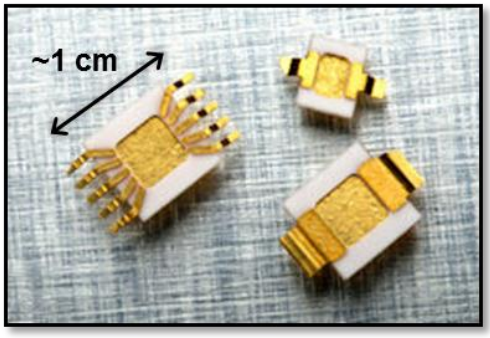


Fig. 1.2 Ceramic (alumina) 1-level package frames with a conductive Cu base and leads used today for high power and high frequency applications (photo source: Materion Corporation).

To build a functional electronic system, several IC's and other electronic devices (passive components, antennas, displays, *etc*.) have to be packed together and connected to each other. This is achieved by second-level (2-level) assembly to a printed circuit board (PCB) as shown in Fig. 1.3. After relying on the traditional through-hole assembly (Fig. 1.3(a)) throughout the first decades of the microelectronics era, a transition to the more compact surface mount assembly (SMA, as in Fig. 1.3(b)) took place in the late 1980's (Tummala, 2001). This was motivated by the increasing number of transistors and terminals of each IC as well as the growing number of IC's in each system. This increasing complexity and the associated size restrictions have also resulted in replacing the traditional DIP with smaller 1-level packages like the quad flat package (QFP) and chip-scale package (CSP) as shown in Fig. 1.3(b,c).

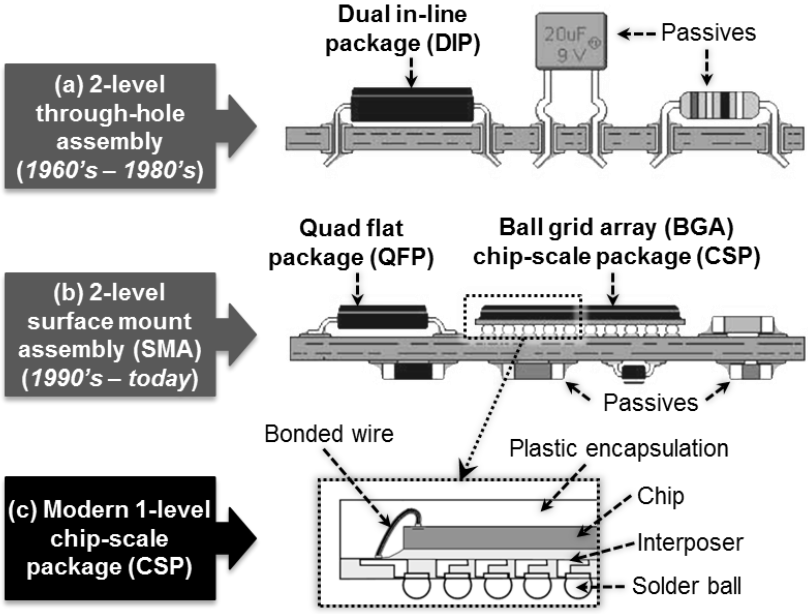


Fig. 1.3 (a,b) Cross-sectional schematics of common 2-level packaging schemes (through-hole and surface mount assembly); and (c) cross-sectional schematic of a modern 1-level chip-scale package (adapted from: Tummala, 2001; Intel, 2000).

A more recent development in electronic packaging makes use of vertical (3D) stacking of several chips within one CSP by means of through-silicon connecting vias to obtain a higher density of devices inside the same package

(Sakuma *et al.*, 2008). Nevertheless, modern IC packaging remains largely dependent on the same conventional principles: connection of a single or multiple chips to an external lead frame through wire bonding, plastic overmolding for chip protection and PCB assembly of different IC's by soldering.

A modern electronic device like the iPhone® 5 smartphone shown in Fig. 1.4 is usually composed of a main PCB in addition to other components like the battery and the display; all sealed in a system-level package (*i.e.*, the front and back covers). The increasing need for efficiency and intelligence in such portable electronic systems has led to an extreme reduction in chip sizes as well as the introduction of a new generation of microsystems known as micro-electro-mechanical systems (MEMS). In the example of Fig. 1.4, MEMS-based microphones and motion sensors (multi-axis accelerometers and gyroscopes) are deployed in order to enhance the awareness of the smartphone of its surrounding acoustic waves as well as its own motion and orientation. Most MEMS chips are small in size and efficient in power consumption. However, they require special protection because of their fragile moving parts that have to be housed in a sealed environment as discussed in the next section.

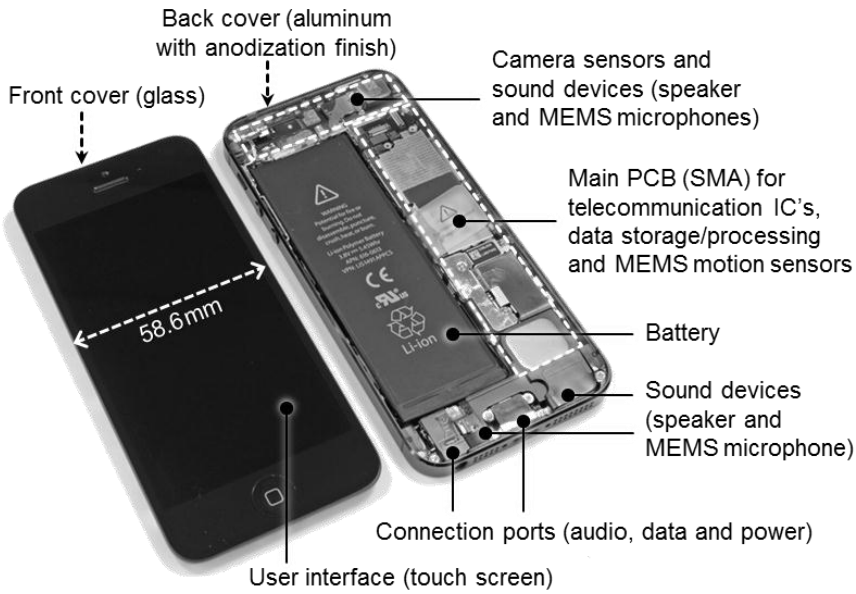


Fig. 1.4 The system-level package (case) and the main components of the iPhone® 5 smartphone produced by Apple Inc. in 2012 (photo source: iFixit.com).

1.2 Packaging requirements of MEMS and advanced microsystems

Micro- and nano-electro-mechanical systems or structures (MEMS and NEMS) are a group of microsystems which commonly feature electrical functionality as well as mechanical parts at the micrometer- and nanometer-scale, respectively. When optical functionality is also involved, the terms micro- and nano-opto-electro-mechanical systems or structures (MOEMS and NOEMS) are eventually used. The range of applications of this group of advanced microsystems is in fact quite diverse as illustrated by the examples in Fig. 1.5 and Table 1.1. Some engineers have gone so far as to construct an electric microcar (Fig. 1.5(a)) or a micro-submarine (Ku *et al.*, 2011) which one day can navigate through the internal organs or blood vessels of a patient to perform ultra-precise tests or treatments. More conventional applications of MEMS include motion sensing using miniature accelerometers (Fig. 1.5(b)) and gyroscopes. Significant efforts have also taken place over the past two decades in the development of advanced microsystems for wireless and electromagnetic systems (see the RF microswitch in Fig. 1.5(c)), as well as for optical and imaging applications (see the micromirrors in Fig. 1.5(d)).

MEMS and other microsystem technologies are closely related to—and dependent on—the more traditional semiconductor technologies for IC's (Nathanson *et al.*, 1967; Witvrouw *et al.*, 2010-A). However, the same cannot be said in terms of packaging as explained hereafter. Moreover, it is practically impossible to develop a universal packaging solution that complies with the diverse characteristics and needs of all existing microsystems, especially MEMS and MOEMS.

Next to the universal requirements of an electronic package like high strength, small size and low cost, particular microsystems impose additional requirements on their respective packaging technique as illustrated in Table 1.1. In terms of connectivity, many advanced microsystems require more than the traditional (low frequency) electrical terminals. An RF waveguide, a transparent optical window and/or a physical (or fluidic) conduction channel are examples of the special interfaces needed for advanced microsystems.

Another distinct feature of mechanical microsystems is their need for a cavity (*i.e.*, free space) to facilitate the operation of their mechanical parts. As shown in Table 1.1, some devices even require a specific (low) pressure or specific gases in their surrounding environment for proper operation. For

example, a microswitch requires a moisture-free and oxygen-free environment to prevent corrosion of its miniature metal contacts (see Fig. 1.5(c)), while a critical pressure of an inert gas should be present for an optimum dynamic response (Rebeiz, 2003). Other issues such as protection from particles, mechanical shock and heat dissipation also belong to the long list of challenges that have to be addressed when developing a suitable package for a new microsystem. This is why packaging has long been the bottleneck in the way of utilizing a number of advanced microsystems at a large scale (Gilleo, 2005).

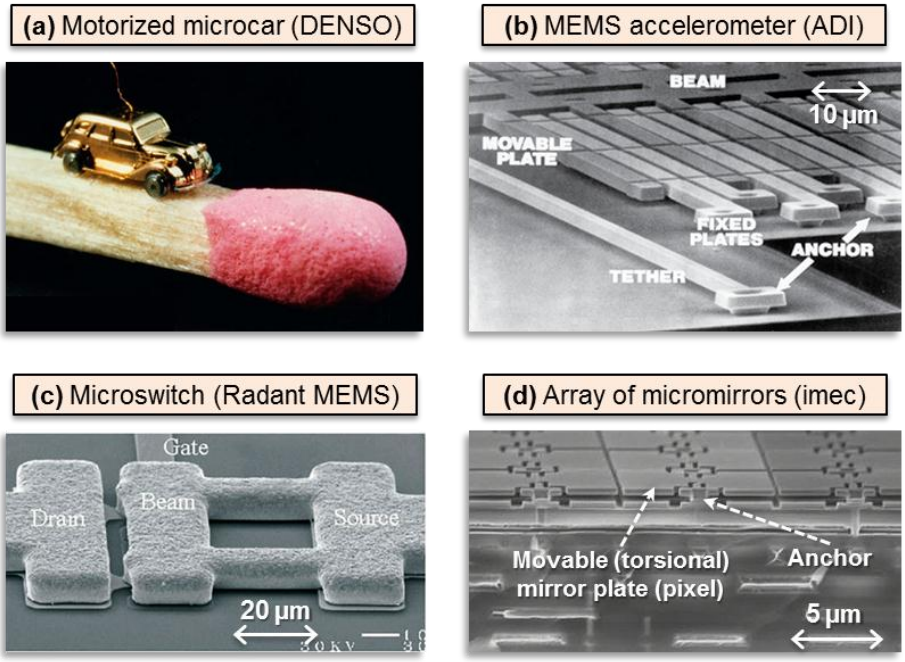


Fig. 1.5 Examples of MEMS and MOEMS: (a) an electric miniature replica (scale 1:1000) of Toyota's first passenger car (PRIME, 2002); (b) an accelerometer for motion sensing applications (O'Reilly *et al.*, 2009); (c) an electrostatically actuated microswitch for wideband RF applications (Majumder *et al.*, 2003); and (d) an array of micromirrors for high-precision UV light projection (Witvrouw *et al.*, 2010-A).

Table 1.1 The main packaging requirements of mechanical microsystems as compared to a traditional IC (data compiled from: Moraja, 2011; Reines and Rebeiz, 2011; Lindroos *et al.*, 2010; Pop, 2010; Knoernschild *et al.*, 2010; Feiertag *et al.*, 2009; Hofmann *et al.*, 2008; Gilleo, 2005; van Spengen *et al.*, 2005; Hsu, 2004; Rebeiz, 2003; He *et al.*, 2000; Buser and De Rooij, 1990).

Device	Application examples	Connections	Internal atmosphere [mbar]	External hazards	Heat dissipation [W/cm^2]
IC (CMOS)	Digital and analog circuits	Electrical	No cavity needed	Moisture, particles	10 – 500
MEMS accelerometer	Motion sensing in portable and automotive systems	Electrical +Mechanical	1 – 500 (design-dependent)	Mechanical shock, moisture, particles	0 (Electrostatic)
Microswitch	Wireless communication and IMOD displays	Electrical (+RF)	1 – 500 (design-dependent)	Moisture, oxygen, particles	0 – 10
Microresonator, gyroscope	Telecommunication circuits, motion sensing	Electrical (+RF) (+Mechanical)	< 0.1	Air, moisture, particles	0 – 0.1
Micromirror	Advanced light projectors and optical communication	Electrical +Optical	< 0.1	Air, moisture, particles	0 – 10
Microbolometer	Thermal and infrared (IR) imaging	Electrical +Thermal/IR	< 0.01	Thermal variations, air, moisture, particles	0 (Thermally isolated)
MEMS pressure sensor	Automotive, portable and biomedical systems	Electrical +Fluidic	0.01 – 1000 (design-dependent)	Mechanical stress, reactive fluids	0 – 10
MEMS microphone	Acoustics (sound and noise sensing)	Electrical +Acoustic	~1000 (air)	Particles, fluids	0 (Electrostatic)
Microfluidic components	Inkjet printing and lab-on-chip (biomedical applications)	Fluidic (+Electrical) (+Optical)	~1000 (gas/liquid)	Particles, reactive biological matter	0 – 10

1.3 Encapsulation techniques

The term *encapsulation* refers here to the cavity formation around a microsystem and the sealing thereof to protect and facilitate the operation of the embedded device(s). In fact, vacuum encapsulation was once the main stream in electronic packaging when electronic rectifiers, switches, amplifiers and displays were all based on vacuum tubes before the invention of transistors and IC's (Kohl, 1951; Wallis and Pomerantz, 1969). These conventional vacuum tubes have established our understanding of small vacuum systems. However, the challenge today is to push the size of vacuum packages to much lower levels in order to exploit the advantages of MEMS and other advanced microsystems. The different techniques developed for (vacuum) encapsulation of modern microsystems are the subject of discussion in this section.

1.3.1 First-level vs. zero-level encapsulation

Among the first commercially available vacuum-encapsulated microsystems were inertial and motion sensors like MEMS accelerometers which were encapsulated using discrete (1-level) packages as schematically illustrated in Fig. 1.6(a). This capping method has been realized using metal packages as done by Analog Devices Inc. (ADI) in the early 1990's (Sherman *et al.*, 1992). Alternatively, ceramic cavity packages have been used by other vendors in the same period (Koen *et al.*, 1995).

Later on, further reduction of the package size has been achieved by making use of various chip- and wafer-level bonding techniques as schematically illustrated in Fig. 1.6(b). Examples of this category of encapsulation processes include anodic bonding (Schmidt, 1998), metallic alloy bonding (Tilmans *et al.*, 2000) and polymer bonding (Jourdain *et al.*, 2003).

Instead of using an external package or cap, both the microsystem and its encapsulating structure can be formed on the same substrate using a monolithic sequence of surface micromachining (or thin film deposition and etching) processes. This relatively new approach is known as thin film encapsulation (see Fig. 1.6(c)). It provides the advantages of a reduced package size as well as direct (on-wafer) protection of the microsystems before any hazardous dicing or handling of the chips takes place. In practice, this means that a protective layer encapsulates the microsystem as soon as its mechanical parts are released and free to move. However, this technique is

still not widely adopted by the industry because of its relative complexity and lower level of maturity. Moreover, the resulting *thin* cap would typically require further mechanical reinforcement by means of plastic overmolding or other 1-level packaging process in order to withstand the shocks and hazards of everyday usage.

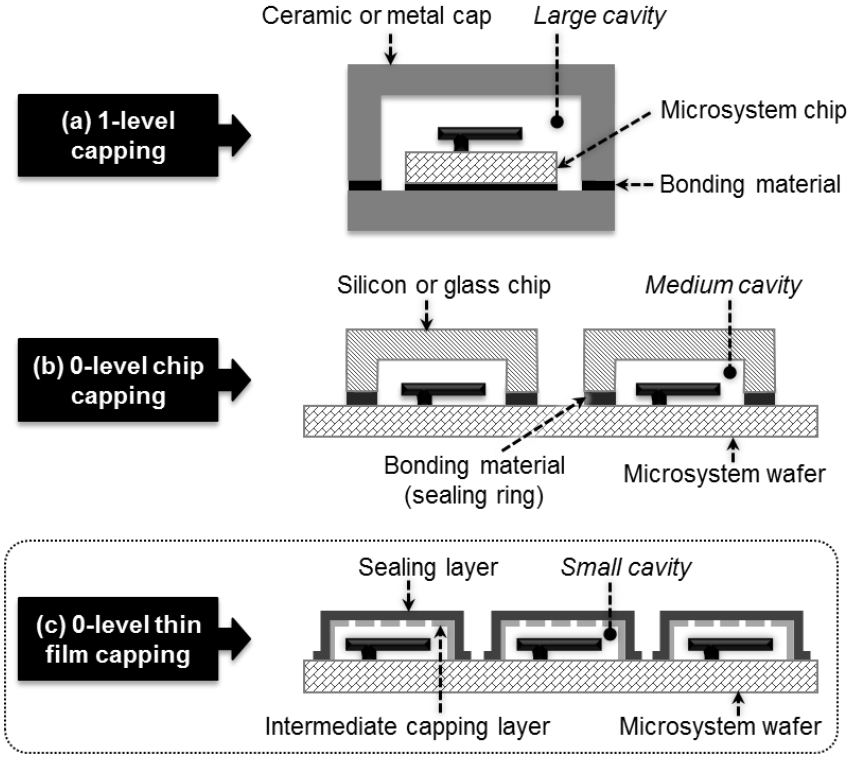


Fig. 1.6 Cross-sectional schematics illustrating the evolution of microsystems encapsulation techniques: from (a) conventional 1-level capping; to (b) 0-level (or wafer-level) chip capping; and finally reaching (c) 0-level thin film capping which offers the highest level of size efficiency.

1.3.2 Thin film encapsulation

Most thin film encapsulation schemes make use of an intermediate capping layer through which a sacrificial material is locally etched to form a microcavity around the encapsulated microsystem as shown in steps (1) and (2) in Fig. 1.7. The microcavities are then collectively closed (or sealed) by depositing a sealing layer on top of the intermediate capping layer in order to

isolate the encapsulated microsystem from its surroundings (step (3) in Fig. 1.7). One of the main functions of the intermediate capping layer is to protect the embedded structure from being contaminated by the sealing material which is deployed by means of a chemical or physical vapor deposition (CVD or PVD) process. The release-etching of the sacrificial layer through the intermediate capping layer can be carried out using planar release channels (Guckel and Burns, 1984) as in Fig. 1.7(a), vertical release holes (Sugiyama *et al*., 1986) as in Fig. 1.7(b) or pores present in the first capping layer (Lebouitz *et al*., 1995) as in Fig. 1.7(c).

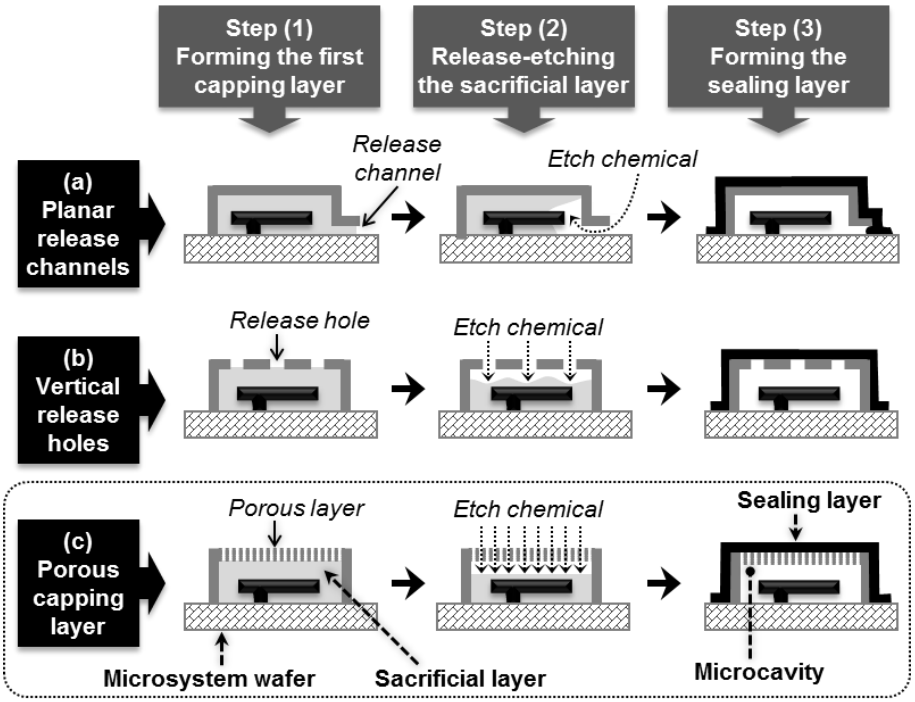


Fig. 1.7 Schematic illustrations of the main processing steps involved in three common techniques for thin film encapsulation. Etching of the sacrificial layer to form a microcavity around the microsystem is performed through: (a) planar release channels at the edge of the capping layer; (b) vertical release holes etched in the capping layer; or (c) a porous membrane used as a capping layer.

An obvious shortcoming of the thin film encapsulation technique based on planar release channels (Fig. 1.7(a)) is the need for an aggressive etching process to be able to form cavities of relatively large lateral dimensions. This

in turn would increase the risk of damaging the structure being encapsulated during the release process. Therefore the first commercial products employing thin film packaging, such as the MEMS resonators of SiTime Corp. (Candler *et al*., 2003; Partridge *et al*., 2005), mostly relied on vertical release holes as in Fig. 1.7(b). The vertical release holes are formed by conventional photolithographic patterning of the first capping layer and are commonly 0.2 to 1.0 µm in width, with an aspect ratio (height to width ratio) of 1 to 10. Despite facilitating faster and easier cavity release, vertical holes present a different challenge: a small amount of the sealing material is deposited inside the microcavity before the holes are closed during the sealing process (Gonzalez *et al*., 2011). This can lead to contamination of the microcavity or an undesired change in the characteristics of the encapsulated microstructure. Therefore, a third technique for thin film encapsulation has been proposed which uses a porous capping layer as shown in Fig. 1.7(c). This technique mitigates the drawbacks of the other techniques based on planar release channels or vertical release holes as discussed in the following subsection.

1.3.3 Porous capping layers

A more recent approach to thin film encapsulation makes use of a porous (or *permeable*) intermediate capping layer as shown in Fig. 1.7(c). A capping layer is considered permeable in this context if it allows the transfer of the gaseous or liquid chemicals and byproducts present during the sacrificial layer release-etching. This is typically possible if the capping layer has physical openings or channels with a smallest dimension in the range of 1 to 50 nm. This approach would facilitate a faster release process compared to the technique based on a planar release channel (as in Fig. 1.7(a)), assuming the porous layer provides direct vertical access to the entire microcavity area (see step (2) in Fig. 1.7(c)). Moreover, contamination of the microcavities is minimized thanks to the rapid closure of the small nanopores during the sealing process. Different porous capping materials have been reported in literature as shown in Table 1.2.

In the 1990's, permeable poly-Si produced by means of an LPCVD process was the first material to be proposed as a porous intermediate cap (Lebouitz *et al*., 1995). Another technique to produce this layer using electrochemical etching was later reported by He and Kim (2007). Despite being inherently compatible with traditional microsystems based on Si, permeable poly-Si suffers from the drawback of requiring high temperature processing (>900 °C). This renders it incompatible with non-Si and above-CMOS microsystems which cannot withstand such high temperatures.

Table 1.2 A comparison between different porous cap materials and the corresponding sacrificial materials reported in literature for thin film encapsulation.

Intermediate capping layer	Literature reference	Production process (and temperature)	Typical thickness	Pore width (and distribution)	Sacrificial materials (and release processes)
Permeable poly-Si	Lebouitz *et al.* (1995, 1999)	LPCVD +anneal (950°C)	<0.2 µm	5 to 20 nm (irregular)	SiO_y (wet HF release)
	He and Kim (2007)	dep. +anneal (1000°C) +electrochem. etch	1.5 µm	5 to 20 nm (regular)	
Permeable polymer (Avatrel)	Monajemi *et al.* (2006)	Spin coating (<120°C)	20 µm	<10 nm (irregular)	Unity polymer (thermally decomposed at 220°C)
Permeable SiOC (Black-Diamond ®)	Verheijden *et al.* (2008)	PECVD (350°C)	<0.2 µm	<5 nm (regular)	SiO_y (HF vapor release)
Porous columnar metal (Cr)	Lee *et al.* (2010)	Sputtering (<100°C)	0.3 µm	<20 nm (vertical channels)	Cu (wet acetic acid + H_2O_2 release)
Permeable poly-SiGe (µc-SiGe)	Guo *et al.* (2012)	PECVD (450°C)	<0.2 µm	<50 nm (irregular)	SiO_y (HF vapor release)
Nanoporous alumina	**Zekry *et al.* (2011)**; Hellin Rico *et al.* (2007)	Al anodization without seed layer (<100°C)	2 to 4 µm	10 to 20 nm (vertical channels)	SiO_y (HF vapor release); polymers (dry O_2-plasma release); a-Si (dry XeF_2 release)
	He and Kim (2006, 2009)	Al anodization +seed layer(s) (<100°C)	1.5 µm	50 nm (vertical channels)	
	Jeon *et al.* (2013)	2-step Al anodization +seed layer (<100°C)	0.4 µm	50 nm (vertical channels)	

During the past decade, interest has significantly increased in thin film encapsulation using porous layers. For example, an encapsulation scheme was proposed by Monajemi *et al*. (2006) based on a system of two polymers: one acting as a permeable cap and the other is used as a thermally decomposable sacrificial material. This scheme uses a relatively low processing temperature (<260 °C) and produces relatively thick caps. However, the polymers used are rather unstable (mechanically and chemically) which raises concerns regarding the overall strength of the cap as well as the cleanness of microcavity after the thermal decomposition process. Subsequently, Verheijden *et al*. (2008) reported another method for thin film encapsulation by making use of permeable SiOC (Black-Diamond®). Being a dielectric material and requiring a process temperature around 350 °C makes this material more compatible with above-CMOS microsystems that operate at high frequencies. One of the drawbacks of this technique is the small thickness of the permeable SiOC layer (<0.2 μm) which imposes the need for a supporting matrix (*i.e.*, another capping layer with lithography-defined release holes). This results in a relatively complex encapsulation process. Another interesting scheme was later reported by Lee *et al*. (2010) based on direct sputtering of porous columnar metal layers such as Cr and Ni at room temperature. Despite the simplicity of this concept, the reliance on a metal layer to form the cap is rather restricting in the case of high-frequency (RF) applications due to the undesired coupling of RF signals to the encapsulating shell.

Two more porous materials have been at the focus of recent research work on thin film encapsulation at imec and KU Leuven (among other institutions), namely microcrystalline poly-SiGe (μc-SiGe) and nanoporous alumina. While μc-SiGe (produced at temperatures close to 450 °C) showed a good compatibility with SiGe-based above-CMOS MEMS technology (Guo *et al*., 2012), it still suffers the drawbacks of a relatively high processing temperature, low strength (need for a supporting matrix with vertical release holes), and low compatibility with RF systems (due to the semiconducting nature of SiGe). The other material under investigation is nanoporous alumina which is the main subject of this thesis. Nanoporous alumina seems to alleviate the drawbacks of other porous capping materials and even provide other interesting advantages as discussed in the following section.

1.4 Nanoporous alumina and thin film encapsulation

It has been known for many decades that anodic oxidation (or anodization) of aluminum-based surfaces in acidic (low-*pH*) electrolytes results in an oxide layer featuring a high density of cylindrical nanopores (Edwards and Keller, 1941; Keller *et al*., 1953; Wada *et al*., 1986). In simple terms, an Al-based surface is oxidized and at the same time vertical channels are etched in the growing oxide during such anodization process. Existing models and experiments suggest that the cylindrical pores tend to form a hexagonal network (as shown in Fig. 1.8) with pore diameter and interval depending on the applied anodization potential as well as the electrolyte composition and the temperature (Parkhutik and Shershulsky, 1992; Thamida and Chang, 2002). It is believed that by choosing the appropriate anodization process conditions (electrolyte, potential and temperature), nanopores with any diameter between 2 and 900 nm, any lateral spacing in the range of 35 to 980 nm and any height from tens of nanometers up to hundreds of micrometers (depending on the process duration) can be produced this way (Chu *et al*., 2006). An example from the literature is shown in Fig. 1.8 for an alumina layer with uniform nanopores prepared in diluted sulfuric acid (10% volume) at 70 V anodization potential and a temperature of 0 °C.

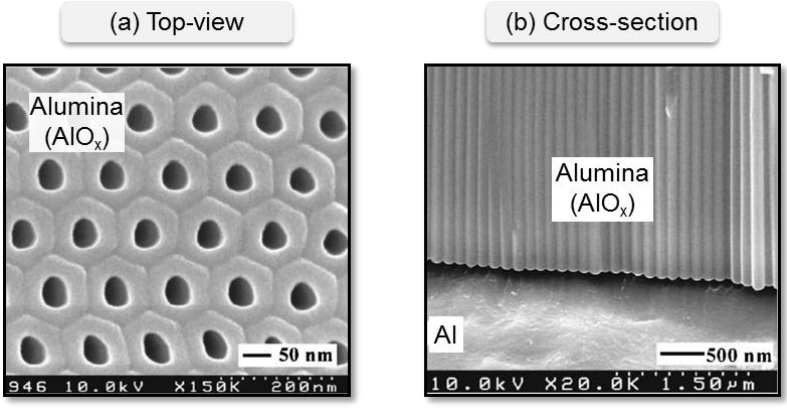


Fig. 1.8 (a) Top-view and (b) cross-sectional SEM of a porous alumina layer prepared by anodizing an Al layer in diluted sulfuric acid at 70 V and 0 °C. The resulting pore diameter is ~50 nm and pore interval is ~130 nm (adapted from: Chu *et al*., 2006).

Being easy to produce, adsorptive of organic coatings, wear- and corrosion-resistant, nanoporous alumina—also known as porous anodic alumina (PAA) or anodic aluminum oxide (AAO)—has steadily been used by large-scale industries (*e.g.*, construction, transportation, *etc.*) as a protective and decorative finish for Al-based structures (Edwards and Keller, 1941; Wernick *et al*., 1987; Thompson, 1997; Siva Kumar *et al*., 1999). Even modern consumer electronic products still rely on an anodization finish to enhance the durability and the appearance of Al-based cases (as in Fig. 1.4). Moreover, PAA has been attracting significant attention in the field of nano-structuring of materials. The distinctive hexagonally distributed cylindrical nanopores of PAA (with very small diameters and high aspect ratios) have been used as templates to grow a variety of nanostructures such as nanowires (Saito *et al*., 1989; Nielsch *et al*., 2000), metal sheets with nanoholes (Masuda and Fukuda, 1995) and carbon nanotubes (Li *et al*., 1999).

In this thesis, nanoporous alumina is used as a capping layer to create on-wafer microencapsulation structures according to the basic process flow shown in Fig. 1.9(a). The motivation to use nanoporous alumina for microsystems encapsulation is based on a number of its unique characteristics, including the following:

- Its low processing temperature (typically <100 °C), resulting in minimal impact on underlying structures;
- The simplicity and low cost of the anodization process to produce thick porous membranes;
- The regularity and high aspect ratio of the nanopores of PAA membranes which facilitate an effective release-etching of the sacrificial layer and fast sealing;
- The flexibility of defining the dimensions of the nanopores (Chu *et al*., 2006);
- Its compatibility with existing IC materials and processes (Al-based interconnects are common in traditional CMOS technologies);
- Its compatibility with RF microsystems thanks to its low dielectric loss (He and Kim, 2009); and
- Its mechanical strength and durability (anodization of Al surfaces is a known technique to improve their scratch- and wear-resistance).

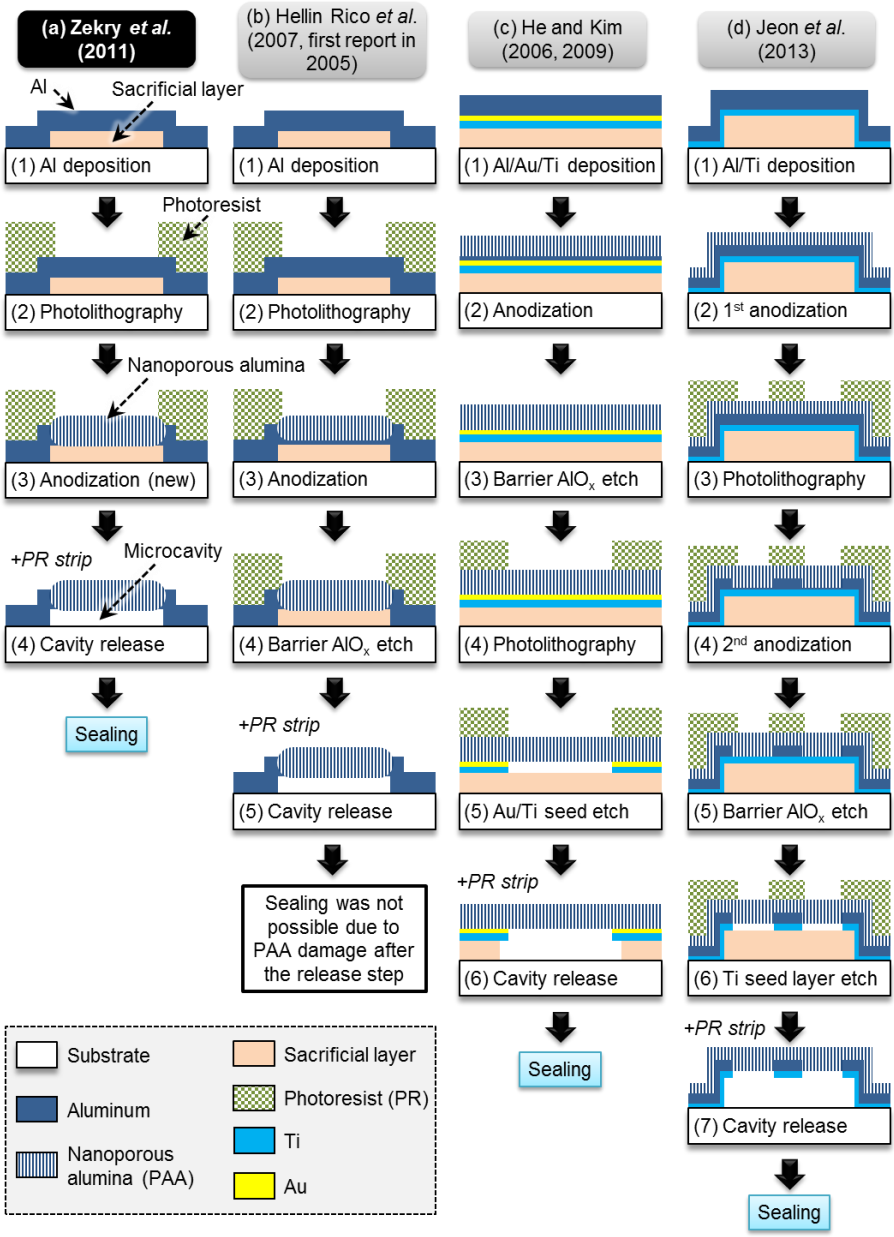


Fig. 1.9 (a) The method used in this work to construct on-wafer microcavities using nanoporous alumina; and (b-d) the other methods reported in literature for microencapsulation using nanoporous alumina.

In February 2005, researchers from imec and KU Leuven filed a provisional patent application describing for the first time a method for encapsulating a device in a microcavity using nanoporous alumina membranes (Witvrouw *et al*., 2010-B). This method was further illustrated by Hellin Rico *et al*. (2007) as shown in Table 1.2 and Fig. 1.9(b). The main processing steps included Al deposition (by sputtering) on top of a sacrificial layer, applying a photoresist mask, anodization of the exposed portion of the Al surface. This is followed by (partial) removal of the thin barrier AlO_x layer remaining at the bottom of the nanopores after the anodization process by means of dry plasma etching. The origin of this thin barrier layer will be discussed in more details in Chapter 2. Next, the photoresist mask is removed and the sacrificial silicon oxide layer is etched through the nanopores of the PAA membranes using HF vapor.

Despite the relative simplicity of the method reported by Hellin Rico *et al*. (2007), it suffered from a number of drawbacks. The direct use of a photoresist mask for the anodization process limits the control on the anodized area (mechanical stresses and chemical reactions may damage the photoresist mask during anodization as explained in Chapter 2). Critical control is also needed for the conditions of the dry etching process to remove the barrier AlO_x layer, thus limiting the reproducibility of this method. Moreover, full release of microcavities with intact PAA membranes could not be achieved, possibly due to insufficient permeability of the PAA membranes and/or incompatibility with the release process used.

Two other schemes for thin film encapsulation using PAA were reported by He and Kim (2006, 2009) and Jeon *et al.* (2013) as shown in Table 1.2 and Fig. 1.9(c,d). In both cases full release and sealing of the microcavities was achieved through PAA membranes with relatively wide pores (around 50 nm in diameter). The barrier AlO_x layer at the bottom of the pores was removed by isotropic wet etching in diluted phosphoric acid. However, as illustrated in Fig. 1.9, both schemes require a more complex implementation (more processing steps) compared to the method of this work (Fig. 1.9(a)). The complexity is mainly caused by the need for the deposition and etching of seed layer(s) underneath the Al layer to guarantee the success of the anodization process. Moreover, applying the anodization process to the full Al surface presents a challenge when scaling such processing schemes to larger substrates (like 200 mm wafers) due to the associated process uniformity issues (He and Kim, 2009), as well as the impractically large electrical current needed. Although the method of He and Kim (2009) produces fully dielectric membranes, it exposes the package anchor to the anodization process, leading

to reduced mechanical stability and hermeticity of the final package. On the other hand, the method of Jeon *et al.* (2013) produces partially conductive membranes, leading to reduced compatibility with RF microsystems.

In this thesis a new method for the formation of the nanoporous alumina membranes and the on-wafer microcavities (Fig. 1.9(a)) will be discussed. This new method significantly reduces the complexity of the encapsulation process and increases the aspect ratio of the nanopores of the capping membrane compared to the schemes reported by He and Kim (2006, 2009) and Jeon *et al.* (2013). Moreover, the novel anodization process reported here addresses the main drawbacks of the processing scheme reported by Hellin Rico *et al*. (2007) by excluding the critical barrier AlO_x layer etching step, as well as by enhancing the stability of the photoresist mask during the anodization step.

If the critical cavity release step shown at the end of the process flows in Fig. 1.9 is performed successfully, all on-wafer microcavities can be sealed simply by depositing—and eventually patterning—any impermeable layer on the wafer (see step (3) in Fig. 1.7). For example, a dielectric or a transparent material can be used for improved compatibility with high frequency (RF) or optical microsystems. In other applications, a semiconducting or metallic layer with very low permeability can be used for sealing if a stable and low pressure is required inside the microcavities (see also the different microsystems packaging requirements in Table 1.1).

1.5 Hermeticity, strength and reliability of thin film packages

One of the most challenging requirements of advanced microsystems packaging is their need for a well-controlled environment inside the package in terms of gas pressure and composition (see Table 1.1). The inherently small sealing structures used in thin film packages make it even more difficult to meet this requirement. This is caused by the short diffusion (or leakage) path of surrounding gas molecules through (or at the edges of) thin caps. Furthermore, devising precise techniques to measure the small gas leakages (*i.e.*, pressure variations) in miniature packages is both necessary and challenging (Moraja, 2011). To understand the significance of gas leakages in micropackages, it is useful to consider the example of a vacuum-sealed thin film package of a typical cavity volume of 1 nl. This package would reach a complete refill with air (or 1 bar pressure increase) after 10 years of its

sealing if the effective air leak rate is approximately 10^{-14} mbar.l/s. Despite its very small value, this leak rate is clearly significant in this example due to the extremely small internal volume of the package.

Besides hermeticity, a thin film package must satisfy a wide range of performance and reliability requirements set forth by the enclosed microsystem and its final application. Generally speaking, the package has to be strong enough to protect the enclosed device from any mechanical loads or shocks it may encounter during its final fabrication steps, handling, storage and operation. A thin film package is however inherently fragile and therefore needs reinforcement for itself as well. To illustrate this, consider a typical thin film package with a cap thickness of 5 µm covering a chip area of 500×500 µm^2. Geometrically speaking, this would be equivalent to having a room of 5×5 m^2 area with a roof that is only 5 cm thick. On top of that, the package would be under a constant hydrostatic pressure close to the atmospheric pressure because it is typically sealed in vacuum. Although the laws of scaling indicate that the micropackage is relatively stronger than a macro-scale structure with the same area to thickness ratio, reinforcement of such thin film package is still needed under relatively large loads. This reinforcement can be achieved by increasing the cap thickness, using stronger materials, reducing the package area and/or introducing special supporting pillars as discussed later in this thesis.

In more demanding applications, the package is also expected to survive different (extreme) thermomechanical or environmental conditions (like high temperatures, pressures or humidity levels). This adds to the list of design and reliability challenges of thin film packages. Testing the actual impact of these extreme loads on micropackages is therefore necessary to verify all design assumptions. Finally, and specifically in high frequency applications, a micropackage should not significantly interfere with the RF signals traveling through an embedded RF device or circuit (Tilmans *et al*., 2010). This imposes certain constraints on the overall package construction and the materials that can be used.

1.6 Objectives of this thesis

In light of the aforementioned historical developments and scientific challenges, the following problem statement can be made:

The continuous miniaturization and extensive commercialization of vacuum-operated microsystems institute the need for new encapsulation techniques that are highly efficient in terms of package size and process simplicity (cost), while maintaining a high level of robustness and connectivity.

It is therefore a main objective of this thesis to develop a simple wafer-level encapsulation process in a controlled environment with minimal package size. This thesis aims at demonstrating that the choice of thin film encapsulation based on nanoporous alumina meets the size and process simplicity requirements of a diverse set of modern microsystems. It is further an objective to develop and employ an optimized set of processes and materials to construct robust wafer-level micropackages. Such processes and materials are intended to be compatible with standard IC wafer fabrication techniques used by the industry today. Furthermore, this thesis aims at investigating the integration of the new encapsulation technology with state-of-the-art microsystems.

Another main objective of this thesis is to develop an effective structural design of the new micropackages. By using a variety of analytical and finite element models, a deep understanding of the thermomechanical characteristics of the new micropackages should be achieved. Another objective is to design and implement robust micropackages and to validate the design assumptions by testing the realized microstructures under different loads.

The final main objective of this thesis is to assess the hermeticity, reliability and RF performance of the new micropackages. This thesis aims at devising precise methods to evaluate the hermeticity of the micropackages and study the impact of the package materials and design on its hermeticity. Furthermore, one of the objectives is to evaluate the reliability of the new micropackages by assessing their survival under extreme thermomechanical and environmental conditions. Finally, this thesis aims at developing micropackages that are compatible with modern RF microsystems. This can be achieved by devising the appropriate package materials and structural design in order to minimize any impact of the package on the RF signals traveling through the encapsulated microstructures.

1.7 Thesis outline

In order to achieve the objectives of this thesis and to discuss the methods used in this research and the obtained results in a structural manner, this

thesis is divided into six chapters including this general introduction. Below is a summary of the contents of the following chapters.

Chapter 2: Technology innovation and integration

This chapter discusses the main (and new) processes and materials developed for the construction of new vacuum micropackages based on nanoporous alumina membranes. First, the basic structure of the micropackages and the main steps used to fabricate them are presented. Next, the major challenges of the encapsulation technology and the innovative solutions developed therefor are discussed, particularly regarding the steps of localized anodization of Al and the formation of on-wafer microcavities. Finally, integration of the encapsulation technology with different microstructures like planar RF transmission lines as well as Ni-based MEMS devices and sensors is investigated.

Chapter 3: Thermomechanical analysis

In this chapter we start with describing analytical and finite element models that are developed to study the thermomechanical behavior of thin film packages based on nanoporous alumina. This is followed by a simulation-based analysis covering the mechanical strength and the impact of temperature variations and residual stresses on the micropackages. Finally, an experimental investigation of the impact of epoxy overmolding (performed at a high pressure and temperature) on the thin film packages is discussed.

Chapter 4: Hermeticity and reliability

This chapter starts with an outline of the main sources of environmental changes in small cavities. Next, the different existing methods to evaluate the hermeticity of micropackages are briefly compared to identify the most suitable techniques for the new thin film packages. This is followed by a detailed hermeticity investigation of the micropackages using an optical detection method of the cap deformation. The feasibility of using miniature pressure sensors that can be embedded inside the micropackages is then discussed. Finally, the results of four different reliability tests applied to the PAA-based thin film packages are presented, providing more insight into the robustness of these microstructures.

Chapter 5: Compatibility with RF microsystems

In this chapter, the compatibility of the encapsulation technology based on nanoporous alumina with RF microsystems is investigated. First, the design principles of a coplanar waveguide that can deliver high frequency signals

across the boundaries of the micropackages are discussed. Electromagnetic simulations are further used to validate the design principle and assess the expected performance. Finally, an experimental investigation is presented where the RF performance of encapsulated transmission lines is measured and compared to an unpackaged (reference) transmission line.

Chapter 6: Conclusions and future work

This chapter provides an overview of the innovative solutions presented in this thesis for the technological, design and testing challenges related to microsystems encapsulation using nanoporous alumina. Additionally, a number of relevant technological and design-related challenges that require further investigation are discussed. Finally, the potential of nanoporous alumina as a microsystems material is highlighted by a few examples of new concepts and applications that can utilize the distinct features of this material.

Chapter 2 Technology innovation and integration

This chapter discusses the main (and new) processes and materials developed for the construction of new vacuum micropackages based on nanoporous alumina membranes. First, the basic structure of the micropackages and the main steps used to fabricate them are presented. Next, the major challenges of the encapsulation technology and the innovative solutions developed therefor are discussed, particularly regarding the steps of localized anodization of Al and the formation of on-wafer microcavities. Finally, integration of the encapsulation technology with different microstructures like planar RF transmission lines as well as Ni-based MEMS devices and sensors is investigated.

2.1 Build-up of a wafer-level encapsulated microsystem

The proposed construction of an on-wafer encapsulated microsystem (or MEMS) using nanoporous alumina is shown in Fig. 2.1. The main structural elements of the micropackage are the microcavity surrounding the encapsulated microsystem, the package anchor (or sealing ring) and the composite cap which is mainly composed of a nanoporous alumina membrane covered by a sealing layer. The lateral dimensions of the microcavity are mainly determined by the size of the encapsulated microsystem (no significant overhead is needed for the package itself). Typical dimensions of microsystems like a microresonator or a microswitch can vary between 50 μm

and 1 mm in the lateral direction, with a typical vertical operation range between 2 and 10 µm.

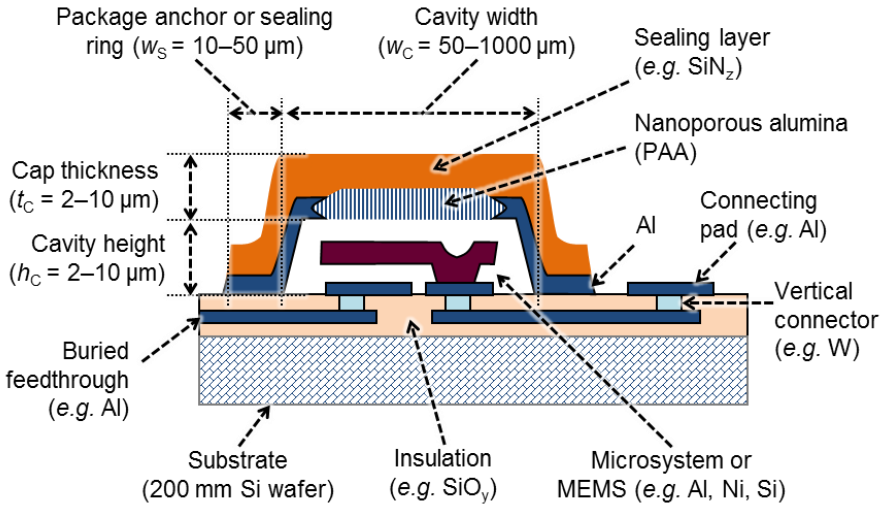


Fig. 2.1 A cross-sectional schematic illustrating the basic construction (materials and dimensions) of a microsystem encapsulated at wafer-level using nanoporous alumina.

The package anchor and the cap are based on an Al layer of a typical thickness of 1 to 3 µm, deposited in a pure form or alloyed with a small percentage (<2%) of another material like Si or Cu. This Al layer is locally converted into a nanoporous alumina membrane within most of the cap area. Leaving the Al layer unaltered at the package anchor has the advantage of better stability and hermeticity compared the situation where the package anchor has a porous base (as in Fig. 1.9(c)). Eventually, supporting pillars that have a similar structure to the package anchor can be introduced within the microcavity to improve the strength of the cap if the package is covering a relatively large area.

The anchor and the cap can be covered by a relatively thick impermeable layer to seal the microcavity. Silicon nitride (SiN_z) is a good candidate as a sealing material because of its good matching in terms of thermal expansion with the silicon substrate, thus reducing the thermally induced stresses in the cap. There are further other advantages of SiN_z as a sealing layer including its mechanical strength, transparency to visible light and low dielectric loss which improves compatibility with RF microsystems. A relatively thick sealing layer should be used in order to provide sufficient hermeticity and mechanical

strength to the cap which typically experiences a differential pressure close to 1 bar (or 0.1 MPa) after being sealed in vacuum (<1 mbar). The final ambient (gas composition and pressure) inside the micropackage is mainly determined by the choice of the gases and pressure used in the sealing layer deposition process. Certain factors may alter the internal ambient of the micropackages after sealing, such as leakage or permeation of external gas molecules as well as outgassing from the internal surfaces of the microcavity. This will be the subject of a more detailed discussion in Chapter 4.

Another important part of the micropackage construction is the electrical interconnects required to deliver the different signals required for the operation of the encapsulated microsystem. Given that the package anchor is partially composed of a conductive layer (Al), an insulating base with embedded interconnects (or buried feedthroughs) is needed to establish a connection between the inside and outside of the micropackage. Vertical interconnects (or plugs) are further needed to reach both the connecting pads and the encapsulated microsystem components as shown in Fig. 2.1.

A number of innovative concepts and fabrication techniques have been developed in order to realize the micropackages described above. This will be the subject of the next sections in this chapter, together with other details about the fabrication steps and materials used to construct the new micropackages and the embedded microsystems.

2.2 Basic encapsulation process flow

The basic processing steps developed to produce sealed on-wafer microcavities (or micropackages) using nanoporous alumina membranes are schematically shown in Fig. 2.2. The process begins with the sputter deposition of an Al layer of 1 to 3 μm thickness on top of a sacrificial layer (situation **(1)**). The choice of the sacrificial material is mainly determined by its compatibility with the encapsulated microsystem and the availability of a process that can be used to etch this material through the narrow pores of the nanoporous alumina membrane. A silicon oxide or a polymer layer can therefore be used, given their known compatibility with existing MEMS technologies and the availability of vapor-based or dry chemical etching processes for them, respectively. The sacrificial layer can be used as deposited in a blanket form (situation **(1-A)**) or it can be patterned in order to obtain well-defined anchors and supporting pillars for the micropackages (situation **(1-B)**).

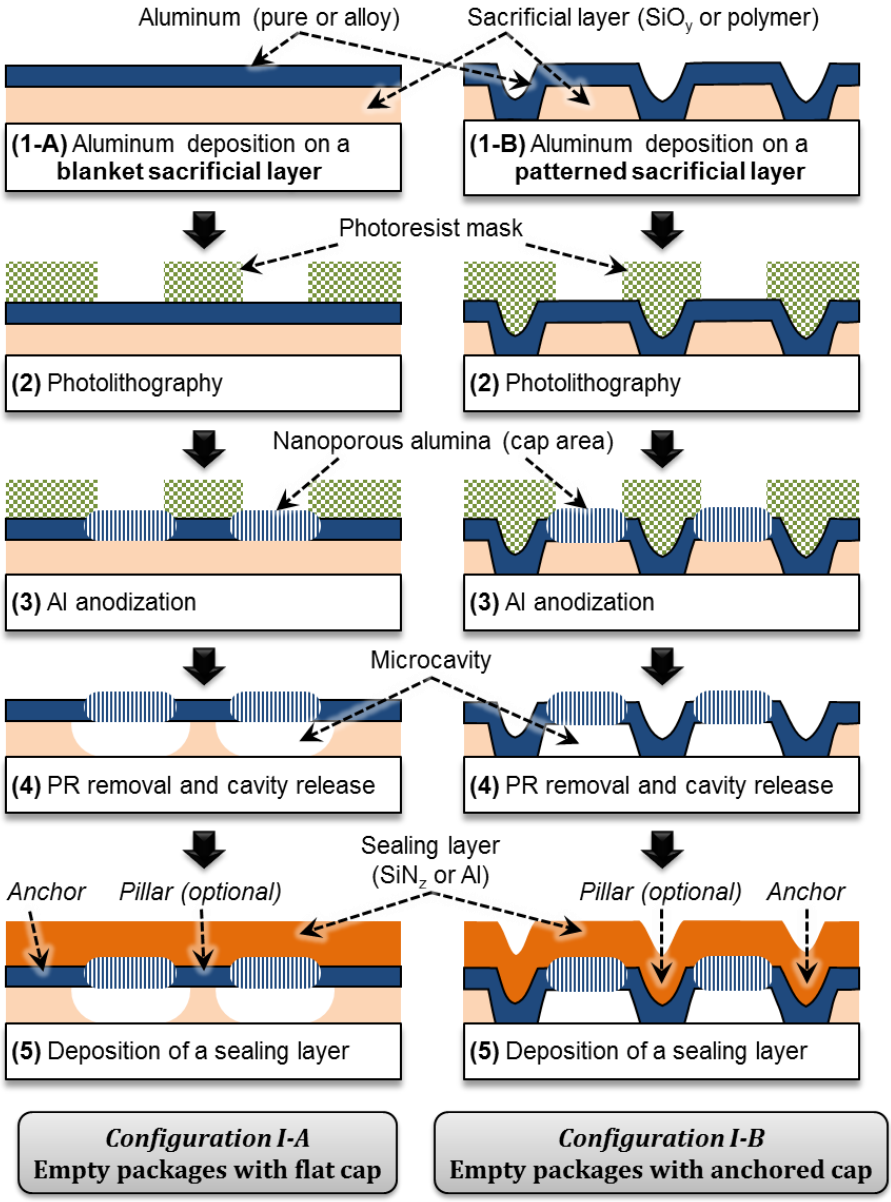


Fig. 2.2 Cross-sectional schematics of the critical processing steps used in creating empty on-wafer micropackages. ***Configuration I-A*** corresponds to the simplest process flow based on one mask and ***Configuration I-B*** corresponds to a process flow based on 2 masks which yields well-defined anchors and pillars for the micropackages.

The formation of the nanoporous alumina membranes begins with a photolithography step to create a mask for the anodization process. This is done using a photoresist layer designated for electrochemical processing with a thickness around 7 µm (situation **(2)**). Next, a specially developed anodization process is performed in diluted sulfuric acid at a temperature close to 30 °C in order to create membranes of nanoporous alumina (situation **(3)**). The new anodization process produces alumina membranes with fully perforated nanopores which facilitate the next etching step of the sacrificial layer to create the microcavities. This eliminates the need for a separate etching step for the removal of the thin barrier AlO_x layer that is typically present at the bottom of nanoporous membranes created using a traditional anodization process. As previously mentioned, this new approach is less complex and more cost-efficient than the other techniques reported so far in the literature for encapsulation using nanoporous alumina (see Fig. 1.9). Creating the microcavities is further achieved by removing the sacrificial layer through the nanoporous membranes by means of a dry or vapor-based etching process (situation **(4)**). Finally, the microcavities are sealed—possibly under low pressure—by the deposition of a relatively thick (>2 µm) impermeable film such as silicon nitride or Al (situation **(5)**). More details about the above mentioned processing steps are discussed in the following sections.

2.3 The technology of nanoporous alumina

2.3.1 New wafer-level anodization process

As discussed in Chapter 1, the anodization of Al-based surfaces in acidic electrolytes is known to produce an alumina (AlO_x) layer featuring a high density of cylindrical nanopores. For the production of nanoporous alumina membranes to form on-wafer microcavities of different shapes, a localized (or masked) anodization process for Al-coated 200 mm wafers has been developed. This process is performed in the electrochemical setup schematically shown in Fig. 2.3(a). This setup was originally manufactured for a standard electroplating process by RENA GmbH, and was later modified at imec 200 mm fabrication facilities to accommodate the anodization process described here. During the anodization process, a fixed potential (typically 20 V) is applied to the Al layer (1 to 3 µm in thickness) on the front side of the wafer as illustrated in Fig. 2.3(b). The value of the anodization potential is chosen to produce nanoporous membranes with a certain pore-to-pore distance (or pitch) as discussed hereafter. A PC-driven high power DC supply

(from Agilent Technologies, Inc.) is used to apply the anodization potential and measure the current flow throughout the process.

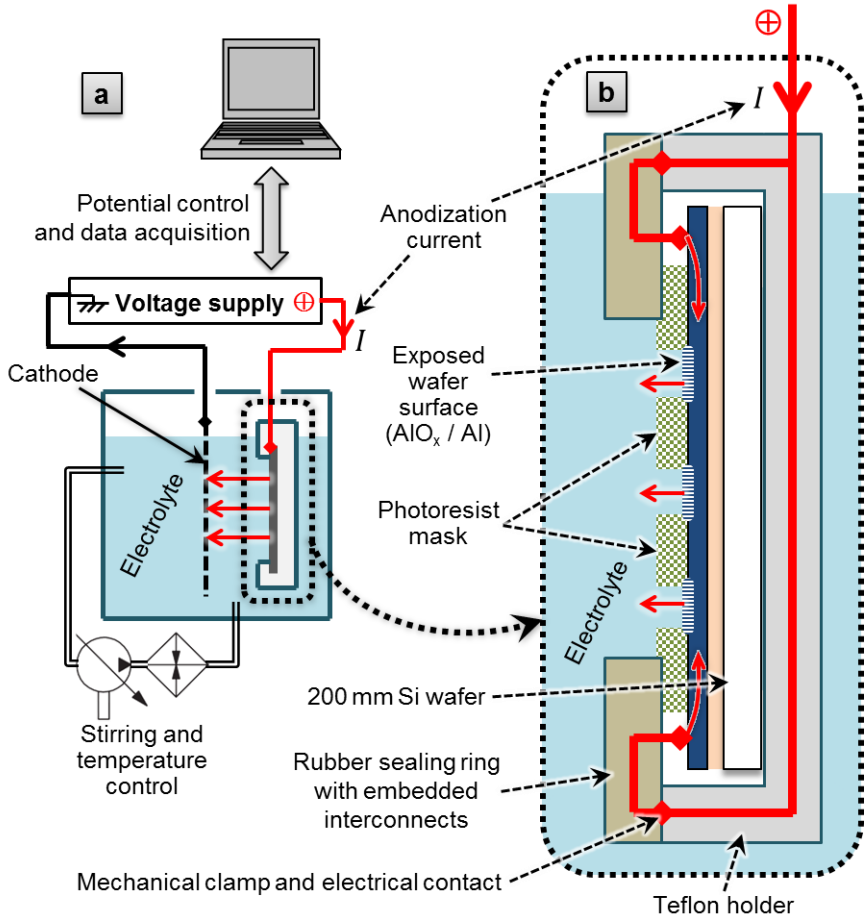


Fig. 2.3 (a) Schematic illustration of the wafer-level anodization setup; and (b) an enlarged cross-sectional schematic showing the current flow through the Teflon holder and the wafer being anodized.

A Teflon-based wafer holder provides the necessary electrical connection to the Al layer on the wafer, while protecting the outer edge (contact area) and the backside of the wafer from the anodization process (as shown Fig. 2.3(b)). The anodization electrolyte is based on diluted sulfuric acid (approximately 10% of acid content in volume), which is constantly stirred and kept at a fixed temperature in the range of 20 to 30 °C. A 7 µm-thick photoresist layer designated for electrochemical processing is used to cover the Al layer, except

at the wafer edge (contact area) and at the locations where a nanoporous alumina membrane (or a microcavity) is to be formed (see situation **(3)** in Fig. 2.2 and Fig. 2.3(b)).

An example of the resulting current density evolution during the wafer-level masked anodization process is shown in Fig. 2.4 together with schematic illustrations of the different stages of the process. As explained for similar anodization experiments in the literature (Moral Vico *et al.*, 2007), the observed changes in the anodization current (or the current density) represent different stages in the PAA formation process. At the beginning of the process, the current rapidly increases in response to the applied potential, given the relatively high conductivity of the Al layer and the acidic electrolyte. The potential is raised gradually from 0 to 20 V at the beginning of the process to avoid a high current (spike) through the system, which may cause damage to the outer surface of the Al layer. Next, the potential is stabilized and the current decreases in response to the formation of a thin barrier alumina (AlO_x) layer on top of the Al layer (situation **(A)** in Fig. 2.4). The current then reaches a certain minimum value corresponding to the largest achievable barrier oxide thickness (this in turn depends on the applied potential which determines the longest distance that can be traveled by the Al and oxygen ions to form the barrier oxide). After that, the current starts increasing again due to the (initially random) perforation of the oxide by the electrolyte which itself is a natural slow etchant of AlO_x (situation **(B)** in Fig. 2.4).

Guided by the required balance in the electric field distribution across the barrier oxide layer, perforations located at a certain potential-dependent distance from each other are more inclined to propagate further into the Al layer (situation **(C)** in Fig. 2.4). Pores that are located at a different interval from this "equilibrium distance" are either merged together or split into multiple pores to reach the equilibrium situation where the electric field distribution follows the pattern shown in Fig. 2.5. This results in a steady propagation of hexagonally distributed cylindrical nanopores within the growing oxide layer (situation **(D)** in Fig. 2.4). The basic electrochemical reactions involved in this process of Al oxidation and localized dissolution are further illustrated in Fig. 2.5. The specific distribution of the electric field inside the barrier (bottom) oxide layer causes the oxidation reaction ($2\,Al^{3+} + 3\,O^{2-} \rightarrow Al_2O_3$) and the dissolution reaction ($Al_2O_3 + 6\,H^+ \rightarrow 3\,H_2O + 2\,Al^{3+}$) to be accelerated at specific locations (mainly the bottom of the pore). The net result of these direction-and location-dependent reactions is a continuous vertical penetration of the hexagonally distributed pores within the growing oxide layer (see also Fig. 1.8).

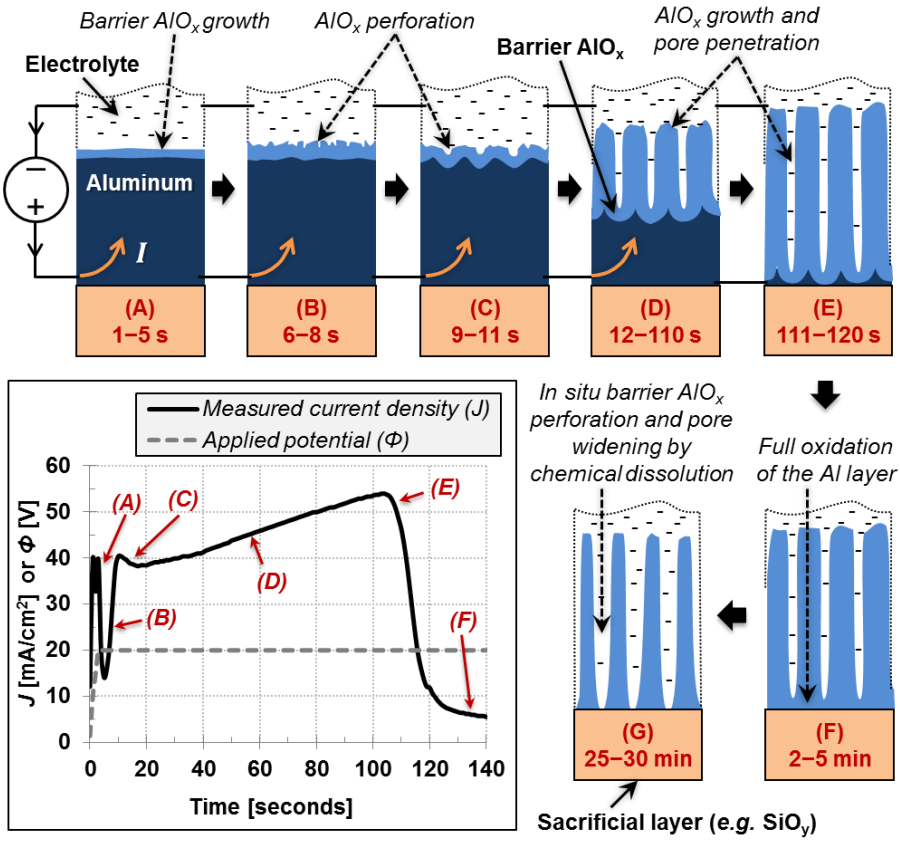


Fig. 2.4 Evolution of the measured current density and the applied potential together with schematic illustrations of the different phases of an anodization process in diluted sulfuric acid. The Al layer thickness is 1.5 µm. The anodization potential and temperature are 20 V and 30 °C, respectively. The current density is obtained as a ratio between the measured total current (*I*) and the theoretical exposed Al area on the wafer which is 20 cm^2 in this case (the remaining Al area is covered by a photoresist mask).

The resulting pore dimensions and distribution are dependent on the anodization process parameters as mentioned earlier. According to Li *et al.* (1998), the pore interval of nanoporous alumina is linearly proportional to the anodization potential with a proportionality factor close to 2.8 nm/V. This means that the expected pore interval in the process mentioned above (20 V anodization potential) is 56 nm, which is close to the values that have been measured using high-magnification SEM (between 50 and 55 nm) as shown

in Fig. 2.6. Furthermore, the pore diameter is dependent on a number of parameters including the *pH* level of the electrolyte, the process temperature and the applied potential. For the anodization process described above (using 10% volume concentration of sulfuric acid at 20 V and 25 °C), the pore diameters were measured using high-magnification SEM and were found to be the range of 10 to 15 nm. Moreover, an expansion in volume (*i.e.*, thickness) occurs when the aluminum layer is converted into nanoporous alumina. The resulting PAA layer is nearly 50% thicker than the starting Al layer and features a high density of nanopores with a very high aspect ratio (>100) as shown in Fig. 2.6.

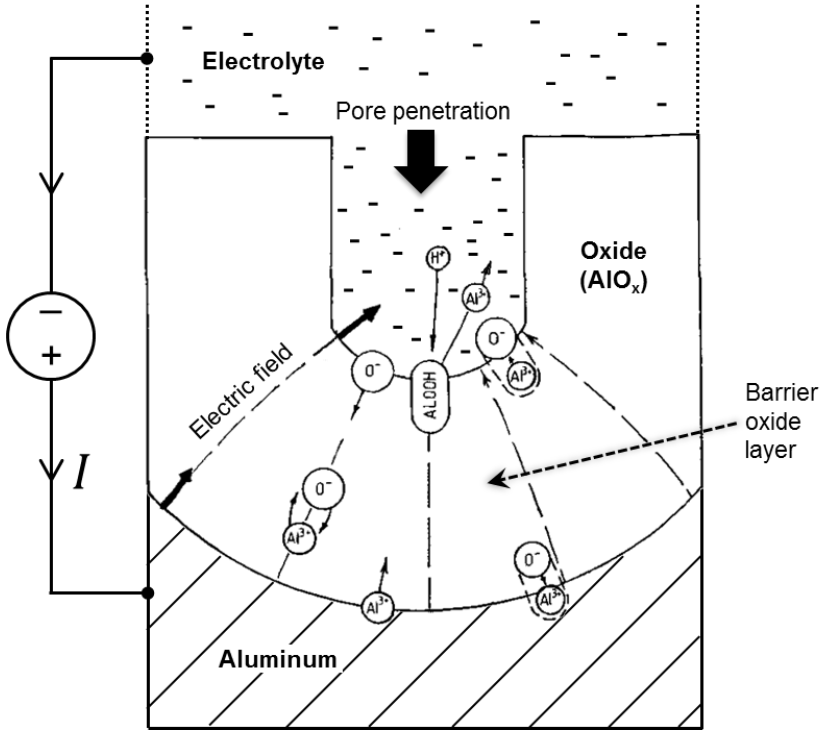


Fig. 2.5 Schematic diagram of the different reactions occurring during Al anodization in an acidic electrolyte. The electric field distribution in the barrier oxide layer and the balance between the different charge flows are the main driver of the vertical penetration and the hexagonal distribution of the pores (adapted from: Parkhutik and Shershulsky, 1992).

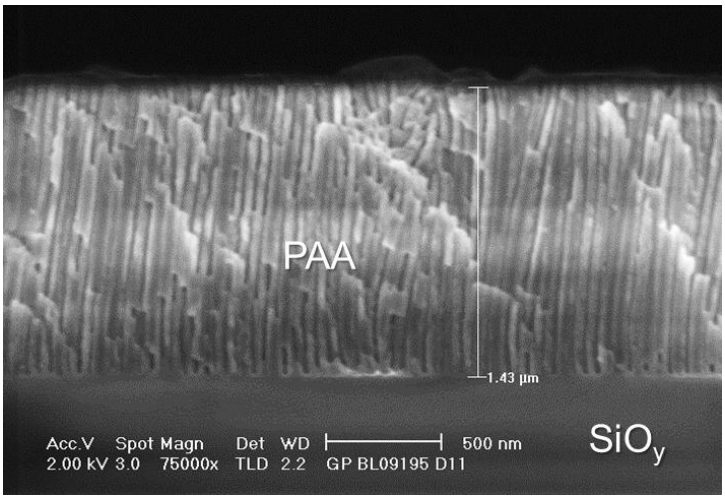


Fig. 2.6 Cross-sectional SEM of the result of masked Al anodization of a 1 µm-thick Al layer on top of a silicon oxide layer. The process is performed in diluted sulfuric acid (10% volume) at an anodization potential of 20 V and a temperature of 25 °C for 3.5 minutes. The resulting PAA layer is approximately 1.5 µm in thickness and features nanopores of 10 to 15 nm diameters with an interval of 50 to 55 nm.

Given that the duration of the high anodization current density phase is approximately 110 s for the anodization process of a 1.5 µm-thick Al layer (as in Fig. 2.4), an estimate of the vertical Al anodization rate of 14 nm/s is obtained for this specific process (using 20 V anodization potential in diluted sulfuric acid at 30 °C). After the phase of steady growth of the nanopores, the anodization current encounters a final decay when the AlO_x layer reaches the interface with the dielectric sacrificial layer (situation **(E)** in Fig. 2.4) causing the conductive current path (*i.e.*, the Al layer) to gradually disappear. This is followed by a mainly chemical oxidation process for any remaining Al underneath the nanopores (situation **(F)** in Fig. 2.4).

Finally, an *in situ* chemical etching process of AlO_x takes place in the anodization electrolyte, yielding slightly wider nanopores (15 to 20 nm in diameter) and a perforated AlO_x barrier layer at the bottom of the pores (situation **(G)** in Fig. 2.4). This *in situ* etching process makes use of the fact that anodization electrolytes used to produce PAA are actually slow etchants of AlO_x at slightly elevated temperatures (Nielsch *et al.*, 2000). To accelerate this *in situ* barrier layer etching, a small amount of phosphoric acid (around 2% of volume concentration) is added to the anodization electrolyte which also contains sulfuric acid at 8% volume concentration. The resulting total

process duration is typically between 25 and 30 minutes, including the time needed to grow the nanoporous layer and achieve the *in situ* barrier AlO_x perforation.

The nanoporous alumina membranes created using this localized anodization process are expected to take the shapes defined by the photoresist mask as discussed hereafter. Producing the nanoporous alumina membranes by localized rather than full anodization of the Al layer provides several advantages, including:

- Eliminating the need for any conductive seed layer(s) by creating a low-resistance path for the anodization current through the masked portion of the Al layer (seed layers are employed in more complex encapsulation processes as previously shown in Fig. 1.9(c,d));
- Limiting the total surface area being anodized and therefore reducing the required electrical current and the associated heating effects when the process is applied to a large substrate (200 mm wafer); and
- Improving the reliability of the produced packages by protecting the anchors and the supporting pillars from the anodization process (see Fig. 2.2).

2.3.2 Improved mask design for localized anodization

The reactions producing nanoporous alumina (or PAA) will always take place as long as an appropriate electrolyte and potential (or current flow) are present at the Al surface. The path of the anodization current and the associated growth of PAA within an Al layer covered by a photoresist mask having a simple opening that defines the cap area (*conventional design*) are illustrated in Fig. 2.7. Initially, the PAA cap structure grows vertically within the area defined by the photoresist mask (width $= w_C$) as shown in Fig. 2.7(a). After this vertical growth phase, the PAA structure continues to grow laterally (distance $= w_E$) beyond the mask-defined edges due to the continuous current supply from the wafer perimeter (see Fig. 2.7(b)).

During the lateral extension of the anodization process, the photoresist breaks off at the edges of the growing PAA structure, mainly due to the volume—or thickness—expansion of the Al layer during its oxidation (around 50%, as observed from Fig. 2.6 and Fig. 2.8). Other potential causes for the photoresist delamination include its attack by the anodization electrolyte or the localized pressure build-up caused by the gaseous byproducts of the

anodization process (mainly the hydrogen produced by the decomposition of water molecules at the Al surface). The lateral dimensions of the resulting nanoporous alumina structures using this *conventional mask design* are dependent on the process duration as discussed later in this section.

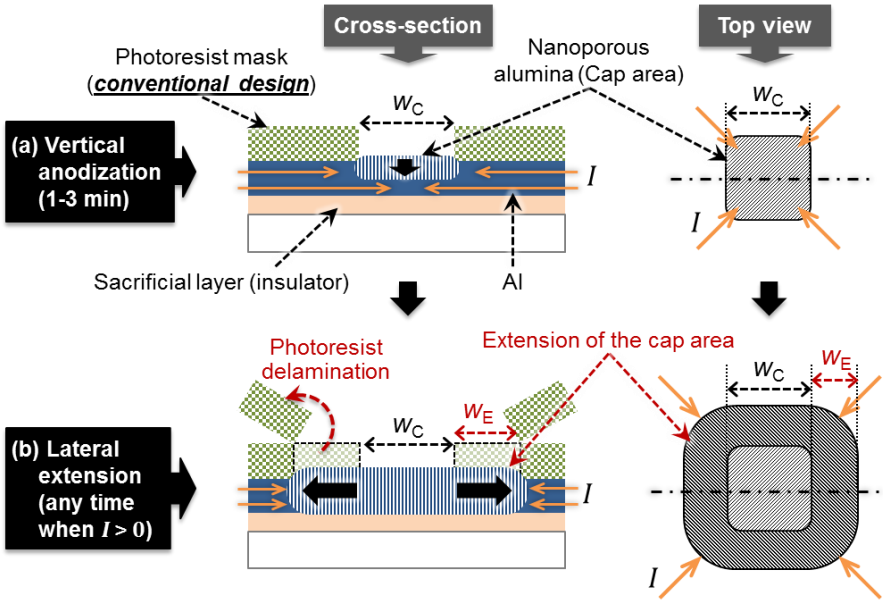


Fig. 2.7 Schematic illustrations of the phases of localized anodization using a *conventional* photoresist mask: (a) Vertical growth of nanoporous alumina within the cap area defines by the mask; and (b) lateral extension of the cap area due to the continuous current flow at the edges of the cap area.

One way to overcome this unwanted lateral extension of the nanoporous alumina structures is to insure that the anodization current supply is terminated once the vertical growth phase ends. This vertical growth phase lasts between 1 and 3 minutes depending on a number of parameters including the exact Al layer thickness, electrolyte composition and potential. Given that all these parameters can vary across a relatively large surface (*e.g.*, 200 mm wafer), a simple disconnection of the anodization current from the whole wafer cannot guarantee a uniform anodization with minimal lateral extension of all structures on the wafer. Therefore, an alternative method is needed to disconnect the anodization current within a small area when the local vertical growth of nanoporous alumina is complete. Such method is described hereafter.

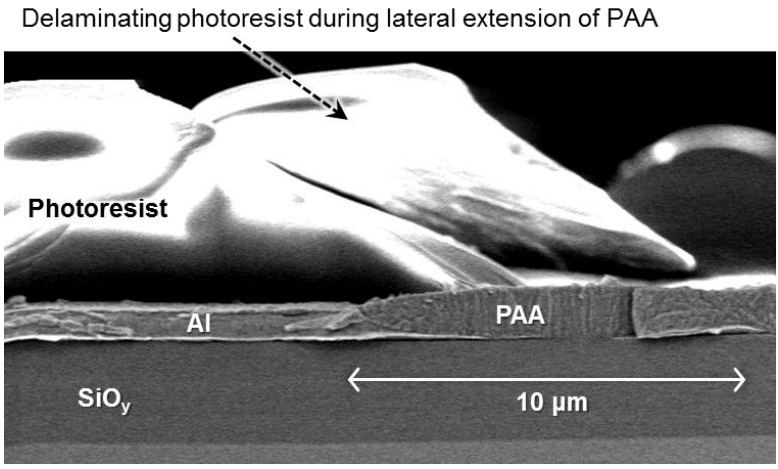


Fig. 2.8 Cross-sectional SEM showing the partial delamination of the photoresist mask during the lateral extension phase of the anodization process as shown in Fig. 2.7(b) (corresponds also to wafer B in Fig. 2.11).

An improved design for the anodization mask has been developed which involves *borderlines* that surround small areas containing groups of the intended nanoporous alumina structures (or caps) as conceptually shown in Fig. 2.9 and Fig. 2.10. In this case, the vertical anodization phase proceeds normally as in the previous case of the *conventional design*, given that the anodization current can reach every point on the wafer through the non-oxidized portions of the Al layer as shown in Fig. 2.9(a) and Fig. 2.10(a). By the end of the vertical anodization phase within the small area shown in Fig. 2.9, the borderline (with width = w_B) is completely anodized and is hence transformed into an insulator (nanoporous alumina). From this point on, the borderline forms a closed insulating loop that prevents the current from reaching any of the enclosed nanoporous alumina structures (caps) as shown in Fig. 2.9(b) and Fig. 2.10(b)—given that the underlying sacrificial layer is also an insulator. Meanwhile, the anodization process can continue in other areas of the wafer where the vertical anodization phase is not complete. Hence, the borderline acts in this scheme as a localized and self-synchronized OFF switch for the anodization current, preventing any lateral extension of the cap area (width = W_C) after the completion of the vertical anodization phase. The lateral extension (for a distance = w_E) takes place only at the outer edge of the borderlines. The nanoporous alumina structures surrounded by the borderline (the cap area) can therefore precisely follow the shape of the photoresist mask, even after a relatively long anodization process.

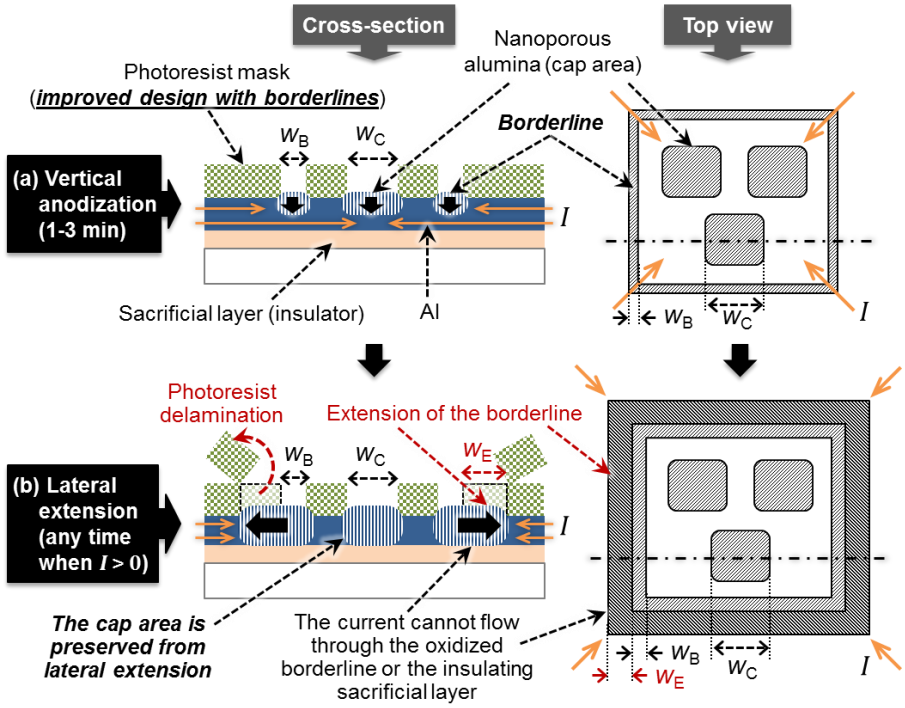


Fig. 2.9 Schematic illustrations of the phases of localized anodization using an *improved design* of the photoresist mask featuring a *borderline* surrounding the cap area: (a) Vertical growth of nanoporous alumina within the cap area and borderline; and (b) lateral extension of the borderline while the cap area is preserved from extension thanks to the oxidized borderline.

The experimental results shown in Fig. 2.11 demonstrate the effectiveness of the improved photoresist mask design compared to the conventional design mentioned above. Three 200 mm wafers (A, B and C) covered with Al layers of approximately 1 µm thickness have been anodized in similar conditions (in diluted sulfuric acid at a potential of 20 V and a temperature in the range of 20 to 25 °C). Two of the wafers (A and B) are covered with a photoresist mask of a conventional design (without borderlines) with a total exposed Al area of approximately 20 cm^2. The third wafer (C) is covered with a photoresist mask of a different design featuring borderlines of 20 µm width (w_B) with a separation of 200 µm between each two neighboring borderlines. The area surrounded by each borderline is approximately 46 mm^2, and the total exposed Al area on wafer C is approximately 55 cm^2.

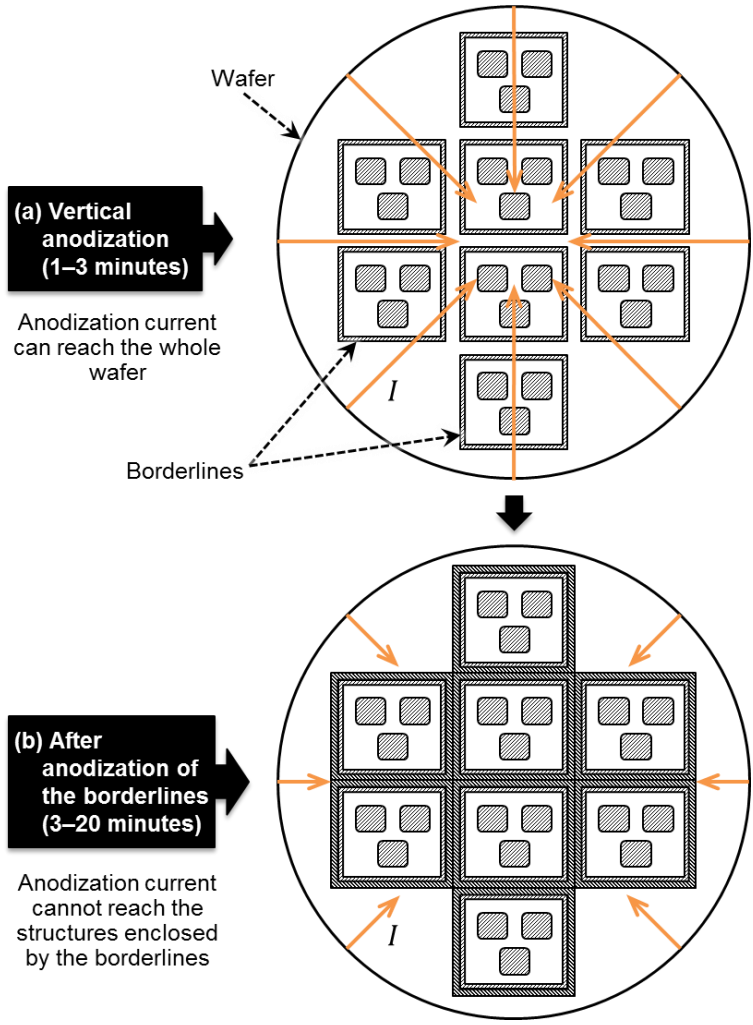


Fig. 2.10 Top-view schematics illustrating the concept of grouping the structures to be anodized on a wafer and surrounding them by borderlines (in the mask design) to prevent lateral extension of the anodization process (dimensions are not to scale).

In the case of the *conventional mask design*, the micrograph in Fig. 2.11(a) shows a lateral extension of 330 µm for a PAA structure of 160 µm width on wafer A where the anodization process duration is approximately 50 minutes. A similar PAA structure on wafer B, where the anodization process duration is only 10 minutes, undergoes a lateral extension close to 50 µm as shown in Fig. 2.11(b). Furthermore, the current density evolution shown

in Fig. 2.11(d) provides more details about the localized anodization process. The vertical anodization phase, which corresponds to the initial peak in the current density (close to 100 mA/cm^2), lasts approximately 2 minutes. This is followed by lateral extension of all the PAA structures on wafers A and B, corresponding to a lower current density that remains until the current is manually switched off. The oscillations in the current density after the vertical anodization phase are attributed to a repeated delamination of small sections of the photoresist mask; periodically exposing more of the Al surface to the anodization electrolyte (see Fig. 2.8). By dividing the total lateral extension (330 μm) by the duration of the final low current phase (approximately 48 min.), an estimate of the lateral PAA growth rate on wafer A can be obtained (6.9 μm/min.). The same calculation for wafer B yields a comparable lateral growth rate of 6.3 μm/min. (50 μm divided by 8 min.).

In the case of the *improved mask design with borderlines* (Fig. 2.11(c)), the situation is rather different. Despite the relatively long anodization process applied to wafer C (20 minutes), inspection of the PAA structures surrounded by a borderline reveals almost no lateral extension beyond the photoresist edge. As shown in the cross-sectional SEM in Fig. 2.11(c), the edge of the photoresist mask clearly defines the transition from Al to PAA with only a thin trace of PAA observed underneath the photoresist mask for a distance close to 6 μm. The current density evolution for wafer C (in Fig. 2.11(d)) further clarifies the dynamics of the anodization process using the improved mask design with borderlines. After the vertical anodization phase—lasting around 2 minutes—a sharp fall in the anodization current density indicates an automatic current cut-off from most of the areas surrounded by borderlines. This is followed by repeated current peaks at a very low level (less than 1 mA/cm^2) indicating photoresist delamination and lateral PAA extension in the small area outside the borderlines (see Fig. 2.10(b) and the top-view micrograph in Fig. 2.11(c)). Given that the separation between neighboring borderlines is 200 μm, the lateral extension of each borderline is possible only for a distance of 100 μm (then all the Al area among the borderlines is oxidized). This fact is also clear from the current density evolution for wafer C which shows a final current cut-off (below 0.1 mA/cm^2) approximately 18 minutes after the end of the vertical PAA growth phase—when the Al surface among the borderlines is fully oxidized. An estimate of the lateral growth rate of PAA outside the borderlines on wafer C is 5.6 μm/min (100 μm lateral extension in 18 minutes). This lateral growth rate is also comparable to the rates observed on wafers A and B (given the similar anodization process parameters).

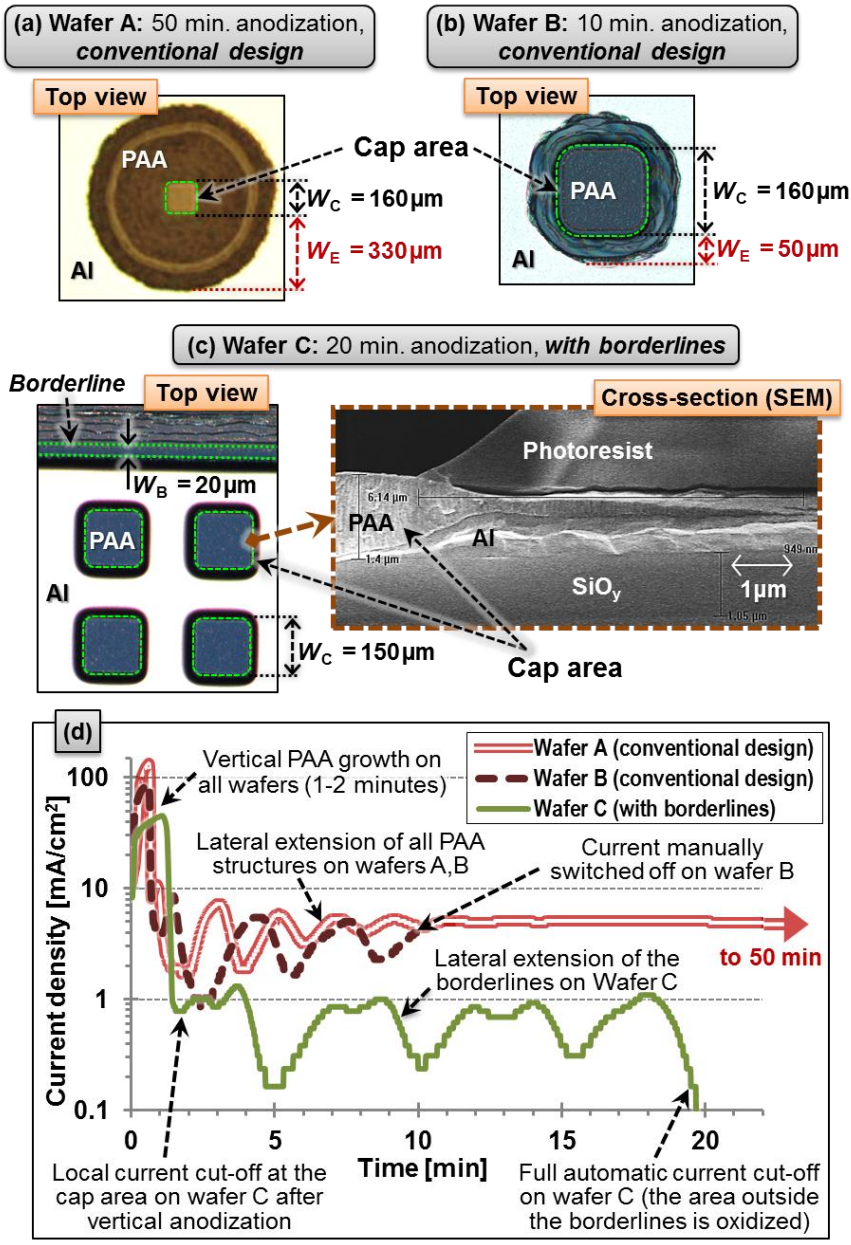


Fig. 2.11 (a-c) Micrographs and (d) the current density evolution of 3 anodization experiments of 1 µm-thick Al layers. Wafers A and B use a conventional photoresist mask (as in Fig. 2.7 and Fig. 2.8), while wafer C uses the improved mask design with borderlines (as in Fig. 2.9).

It is therefore clear that the *improved mask design with borderlines* eliminates the need to critically control the duration of applying the anodization current to achieve minimal lateral extension of the nanoporous structures. Moreover, wafer-dependent and time-dependent variations in the anodization process parameters are automatically compensated with this improved mask design, resulting in a more robust and reproducible wafer-level anodization process.

2.4 Formation (release) of the microcavities

The nanoporous alumina membranes created on top of a sacrificial layer (*e.g.*, silicon oxide or photoresist) can be used to form a large number of microcavities at wafer-level using a release process. Such release process involves selective etching of the sacrificial layer through the nanoporous membranes as previously shown in Fig. 2.2. An important requirement for a successful cavity release is having sufficient permeability of the nanoporous alumina membranes during the etching process of the sacrificial layer. This means that the reactive etchants of the release process should be able to travel through the nanopores of the alumina membranes towards the microcavities being formed, and the byproducts of the dissolution of the sacrificial layer should be able to flow out of the microcavities through the nanopores. This is the motivation for introducing the *in situ* barrier AlO_x perforation to the anodization process as described earlier (see situation (G) in Fig. 2.4).

If the anodization process duration is not long enough to realize the *in situ* barrier AlO_x perforation, then the release process cannot be successfully performed as shown in Fig. 2.12(a,b). However, if the nanoporous alumina membranes are produced with sufficient permeability (by extending the exposure of the wafer to the anodization electrolyte), a large number of on-wafer microcavities can be formed by selectively etching the sacrificial layer through the nanoporous membranes. For instance, a 3 μm-thick SiO_y sacrificial layer is completely removed by exposing the wafer to HF vapor in a reduced-pressure chamber for 120 minutes, yielding freestanding nanoporous alumina membranes of various shapes and sizes (up to 1×1 mm^2) as shown in Fig. 2.12(c).

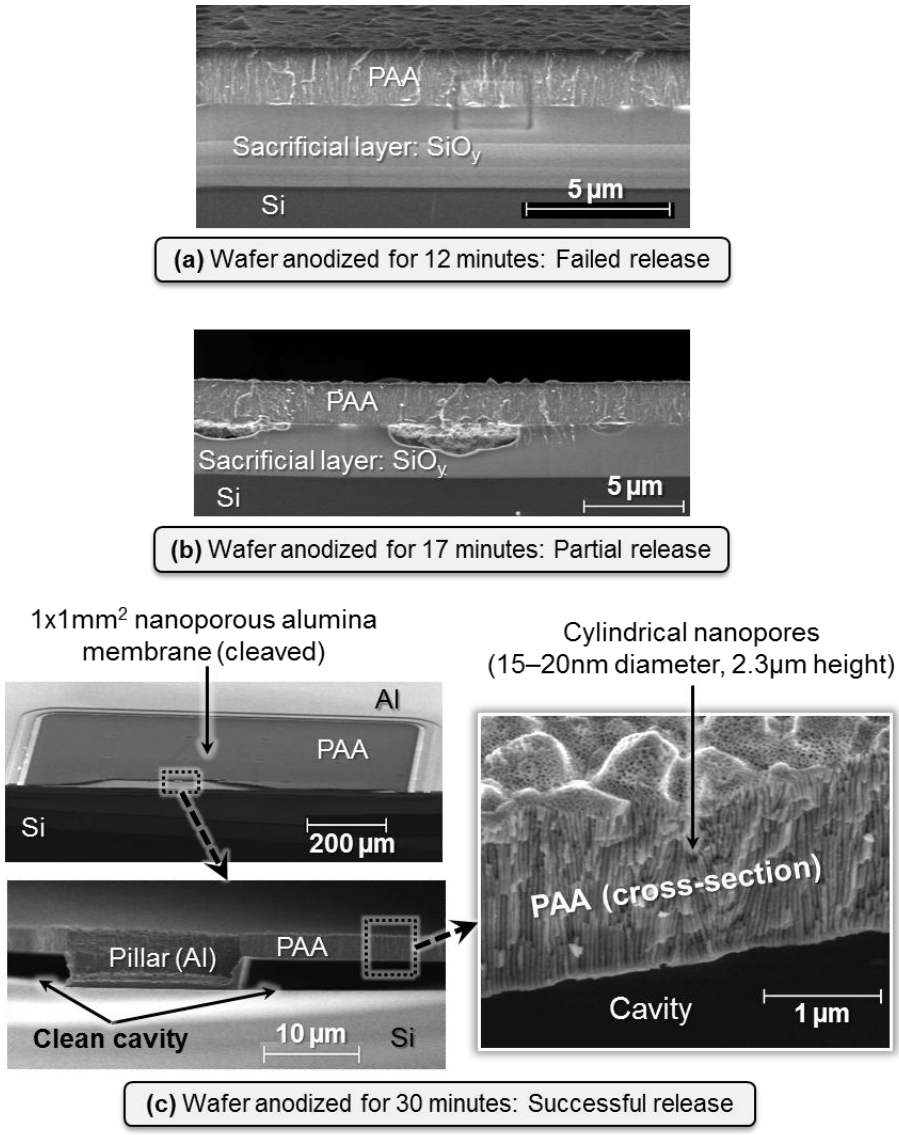


Fig. 2.12 SEM views of three different samples after the HF vapor release-etching of a 3 µm-thick SiO_y sacrificial layer underneath 2.3 µm-thick PAA membranes produced by Al anodization in diluted sulfuric acid for a duration of: (a) 12 minutes; (b) 17 minutes; and (c) 30 minutes. Full release of the microcavity was achieved only in (c) where the anodization process was long enough to realize the *in situ* perforation of the thin barrier AlO_x layer at the bottom of the PAA membranes.

In an HF vapor etching process, an ionization agent containing OH^- ions is needed to ionize the HF molecules before reacting with the silicon oxide (SiO_2) layer, yielding the following reactions at the silicon oxide surface (Lee *et al.*, 1996):

$$4HF_{(ads)} + 2M_{(ads)} \rightarrow 2HF_{2\,(ads)}^{-} + 2MH_{(ads)}^{+} \tag{2.1}$$

$$SiO_{2(s)} + 2HF_{2\,(ads)}^{-} + 2MH_{(ads)}^{+} \rightarrow SiF_{4(g)} + 2H_2O_{(ads)} + 2M_{(ads)} \tag{2.2}$$

where M is an ionizing agent such as water (H_2O), methanol (CH_3OH) or ethanol (C_2H_5OH). From reactions (2.1) and (2.2) it is clear that most of the byproducts of the etching process (H_2O and M) are themselves ionizing agents that may further accelerate the reaction (by positive feedback) if the process conditions provide sufficient HF molecules and allow these ionizing molecules to remain adsorbed at the oxide surface. Lee *et al.* (1996) further analyzed the etching process and proposed the following expression for the oxide etch rate (ER, or the amount of oxide thickness removed per unit time) as a function of the temperature (T) as well as the partial pressure (P) and the vapor pressure (P_v) of HF and the ionizing agent:

$$ER = k_o e^{\frac{\epsilon_R}{T}} \left\{ \frac{\left(\frac{P}{P_v}\right)_{HF}}{\left[1-\left(\frac{P}{P_v}\right)_{HF}\right]\left[ae^{\frac{\epsilon_{HF}}{T}}+\left(\frac{P}{P_v}\right)_{HF}\right]} \right\}^2 \left\{ \frac{\left(\frac{P}{P_v}\right)_{M}}{\left[1-\left(\frac{P}{P_v}\right)_{M}\right]\left[be^{\frac{\epsilon_M}{T}}+\left(\frac{P}{P_v}\right)_{M}\right]} \right\} \tag{2.3}$$

where k_o, a, b, ϵ_R, ϵ_{HF}, and ϵ_M are empirical constants obtained by fitting this equation to experimental data.

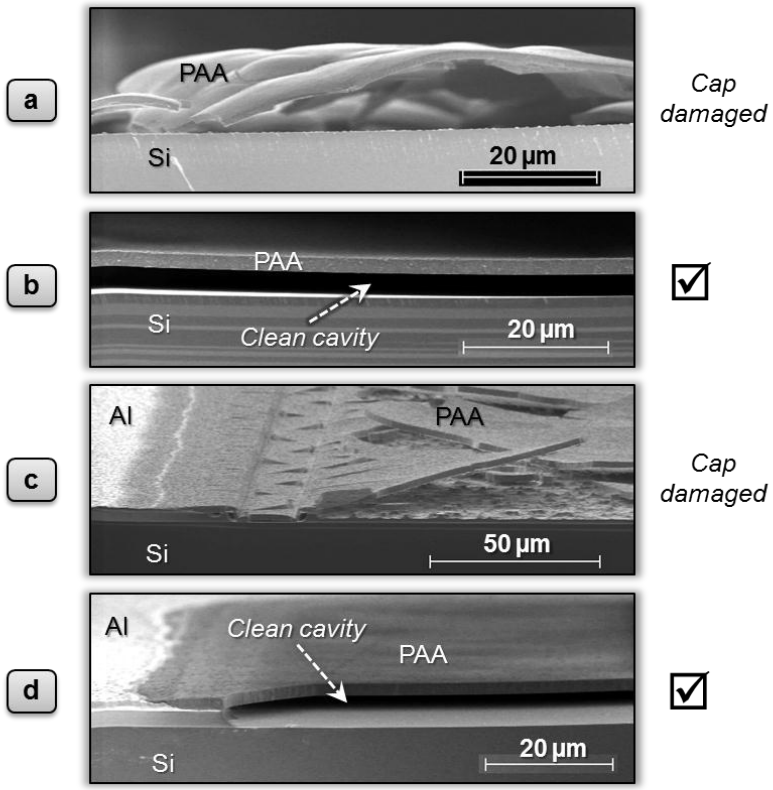
The amount of water and HF present during the cavity release process is critical due to the fact that nanoporous alumina (the cap) can be dissolved in hydrous HF (Chen *et al.*, 2005). The amount of water produced and accumulated during the release process can be significant in certain cases as previously mentioned. Furthermore, equation (2.3) indicates that the etch rate (and the rate of water production in the process) can also be influenced by the temperature, the partial pressure of HF, as well as the type and pressure of the ionizing molecules.

As shown in Fig. 2.13, experiments for the release-etching of silicon oxide using HF vapor have been carried out in two different etch tools: one based on water as an ionizing agent (Gemetec); and the other uses ethanol as an ionizing agent at a relatively higher temperature and lower pressure (Primaxx). When using water as an ionizing agent (in Gemetec tool), failure of the release process (*i.e.*, cap damage) occurs as shown in Fig. 2.13(a) due to

excessive water accumulation. This can be attributed to the reduced water ventilation of this etch process which is performed at a relatively low temperature (35 °C) and high chamber pressure of 0.84 bar (boiling point of water in this pressure is close 95 °C). The cap damage in this kind of release process can be avoided by introducing additional ventilation steps (each lasting more than 2 minutes) during the etch process to reduce water condensation or adsorption as proven by the result in Fig. 2.13(b). However, introducing the ventilation steps limits the etch rate acceleration mentioned earlier, resulting in a much longer process duration (more than 120 minutes instead of 30 minutes).

When using ethanol as an ionizing agent, increasing the temperature to 45 °C, and reducing the pressure to 0.13 bar (in Primaxx tool), the accumulation of water at the surface of nanoporous alumina is expectedly lower (boiling point of water at 0.13 bar pressure is close 52 °C). However, cap damage still takes place if a substantial amount of HF molecules is used as shown in Fig. 2.13(c). By improving the ventilation (further reducing the pressure to 0.1 bar) and reducing the amount of HF used, successful release is achieved in the ethanol-based etch process (with a relatively short process duration) as shown in Fig. 2.13(d). Further reduction of the release process duration can still be achieved by fine tuning other process parameters like the wafer temperature and amount of inert gas (N_2) used.

It is worth mentioning that similar residue-free microcavities have also been obtained using a photoresist (polymer) sacrificial layer which is release-etched using a standard dry oxygen plasma process. Here the only necessary condition for a successful release process is sufficient permeability of the nanoporous alumina membranes as previously indicated for the HF vapor process. The advantages of photoresist as a sacrificial layer are mainly the simplicity and low temperature of its deposition and etching processes. However, the main drawbacks of photoresists (and polymers in general) are their substantial outgassing and their relatively low thermal and chemical stability, resulting in less-clean microcavities and a limited choice of the materials and processes that can be subsequently used in the encapsulation flow.



Sample	Etch tool (gases used)	Wafer temperature	Chamber pressure	Flow ratio HF:M	Duration (x steps)	Result
a	Gemetec (N_2 + HF + M = H_2O)	35 °C	0.84 bar	1 : 1 (not monitored)	30 min. (x 1)	Cap damaged
b					10 min. (x 12)	Release OK
c	Primaxx (N_2 + HF + M = C_2H_5OH)	45 °C	0.13 bar	1 : 1	1.5 min. (x 8)	Cap damaged
d			0.10 bar	0.86 : 1	60 min. (x 1)	Release OK

Fig. 2.13 The results and process parameters of 4 different tests for the removal of 3 µm-thick silicon oxide through nanoporous alumina membranes using HF vapor. The tests are performed in two different etch systems: one based on water (a,b) and the other is based on ethanol (c,d) as an ionizing agent.

2.5 Sealing the microcavities

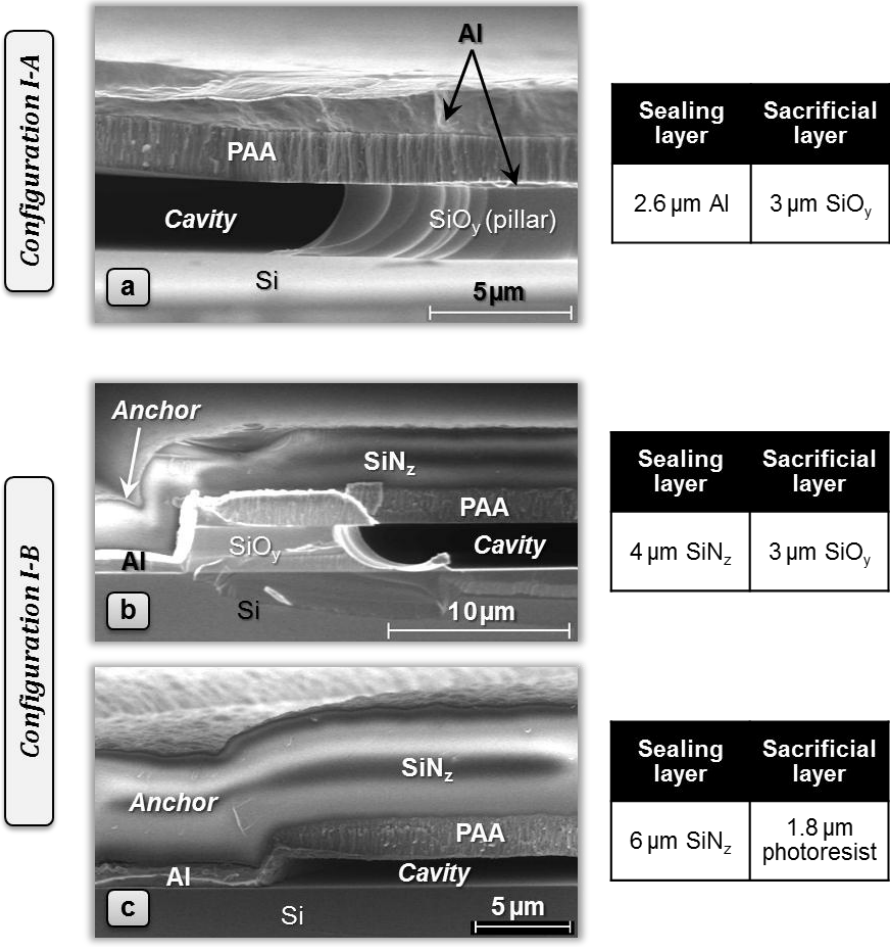
The on-wafer microcavities created by the release of nanoporous alumina membranes can be sealed using any wafer-level physical or chemical deposition process. In Fig. 2.14, three different examples are shown for empty micropackages (corresponding to *Configurations I-A* and *I-B* as previously illustrated in Fig. 2.2). The micropackages in Fig. 2.14 are all based on similar nanoporous alumina membranes of approximately 2.3 µm thickness with cylindrical nanopores of 15 to 20 nm diameter. These microstructures are realized by making use of silicon oxide (SiO_y) or photoresist (PR) as the sacrificial layer in combination with silicon nitride (SiN_z) or Al as the sealing layer. The release process is either based on HF vapor etching for SiO_y or dry oxygen plasma etching for PR as discussed in the previous section. The silicon nitride sealing layer is deposited by means of a PECVD process at 250 °C and a chamber pressure of 6.3 mbar (process gases are SiH_4 and NH_3), whereas sealing by aluminum is performed using a sputter-deposition process at 350 °C at a pressure close to 0.01 mbar (process gas is Ar).

Thorough SEM inspection after the sealing process using either SiN_z or Al revealed no visually observable deposition of the sealing material inside the microcavities. This is attributed to the very narrow and high aspect ratio of the nanopores of the PAA membranes (height to diameter ratio of the nanopores is typically more than 100). These nanopores are rapidly closed at the beginning of the sealing process thus preventing any significant deposition inside the cavity. Any microsystem being encapsulated in this manner is therefore well protected from contamination by the sealing material. A relatively thick (2 to 6 µm) sealing layer is typically needed in order to provide the necessary mechanical strength to the micropackages as discussed in Chapter 3.

A dielectric material (PECVD SiN_z) is chosen as the main sealing layer for the following reasons:

- The established knowledge of PECVD SiN_z deposition techniques;
- The ease of depositing thick layers (*i.e.*, 2 to 10 µm) with a relatively low residual stress (*i.e.*, less than 100 MPa);
- The high quality of PECVD SiN_z (in terms of mechanical and electrical properties) which is commonly used as a passivation layer in traditional IC technologies (Claassen *et al.*, 1985; Lauinger *et al.*, 1996);

- Compatibility with RF microsystems, thanks to the low RF losses of nanoporous alumina (He and Kim, 2009) and PECVD SiN_z (Ng *et al.*, 2003); and
- Compatibility with optical microsystems, given the optical transparency of both PAA and PECVD SiN_z thin films.



Sealing layer	Sacrificial layer
2.6 µm Al	3 µm SiO_y

Sealing layer	Sacrificial layer
4 µm SiN_z	3 µm SiO_y

Sealing layer	Sacrificial layer
6 µm SiN_z	1.8 µm photoresist

Fig. 2.14 Cross-sectional SEM views of three empty thin film packages based on 2.3 µm-thick PAA membranes realized by making use of (a), (c) silicon oxide or (b) photoresist as a sacrificial layer in combination with (a), (b) PECVD silicon nitride or (c) sputtered Al as a sealing layer. The difference between *Configuration I-A* and *I-B* is illustrated in Fig. 2.2.

The use of a metal sealing layer (such as sputtered Al) instead of silicon nitride is expected to enhance the hermeticity of the produced micropackages (Traeger, 1977). However, when used as a final sealing layer, a metallic thin film still suffers from certain drawbacks—compared to a dielectric layer like PECVD SiN_z—including susceptibility to corrosion, relatively large residual stress and low resistance to mechanical scratching and plastic deformations. The physical damage that can take place when sealing a relatively large package (supported only at the edges) at a high temperature (350 °C) using Al is shown in Fig. 2.15(a). The use of a dense grid of supporting pillars, as in Fig. 2.15(b), can mitigate the impact of the high residual stress in the layer but it may not be viable for certain microsystems with large footprints.

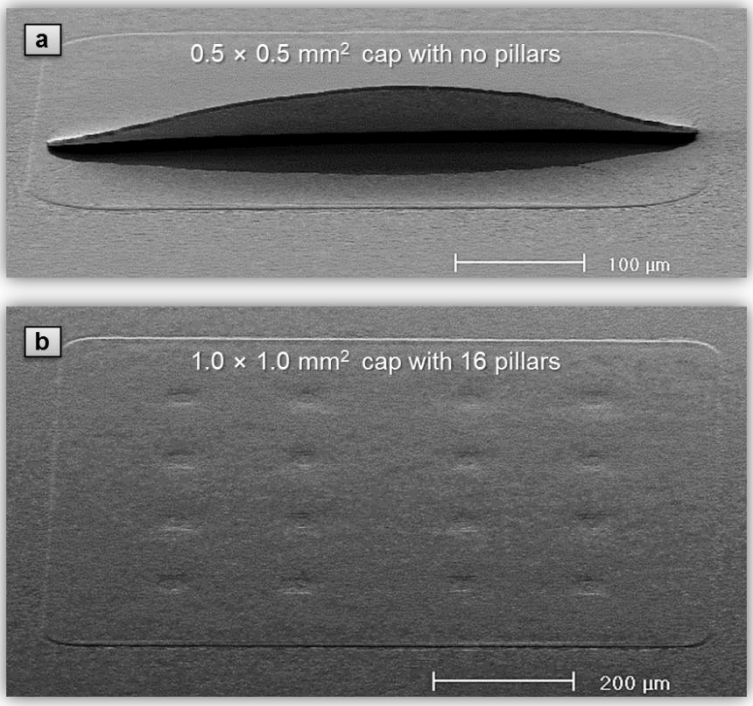


Fig. 2.15 SEM views of two square-shaped packages after sealing with 2.6 µm-thick Al layer at 350 °C: (a) a package of 0.5 x 0.5 mm^2 area with no supporting pillars is torn due to the relatively high tensile stress in the sealing layer; and (b) a larger package of 1 x 1 mm^2 area is still intact thanks to the presence of 16 supporting pillars.

For a theoretical estimation of the internal package pressure at room temperature after sealing, we can use the ideal gas law for a sealed container with a fixed volume (P/T = constant); where P is the gas pressure inside the container and T is the gas temperature. Given that the process pressure is 6.3 mbar at 250 °C (T = 523 K) for PECVD nitride sealing, the final pressure would be around 3.5 mbar (or 350 Pa) at room temperature (T = 293 K). Here it is assumed that the cavity volume and the number of gas molecules inside the cavity do not change after sealing—*i.e.*, no reactions, leakage or outgassing take place immediately after the sealing process. Similarly, for the Al sealing process at an Ar pressure of 0.01 mbar and a temperature of 350 °C (T = 623 K), the final Ar pressure at room temperature is estimated around 0.005 mbar (or 0.5 Pa). It is worth mentioning that no measurement of the actual pressure inside the microcavities could be performed. However, a detailed study of the hermeticity of the micropackages and an investigation of microsensors that can be used for the internal pressure measurements (if integrated inside the microcavities) are discussed in Chapter 4.

2.6 Wafer-level encapsulation of planar RF transmission lines

In order to evaluate the compatibility of the packaging process with existing microsystems technologies and to house test structures inside the thin film packages, the processing schemes illustrated in Fig. 2.16 have been implemented. The main purpose of this process is to encapsulate planar RF transmission lines (like coplanar waveguides, or CPW's) at wafer-level using thin caps based on nanoporous alumina membranes and silicon nitride sealing. In order to achieve this, two levels of Al-based planar interconnects are integrated with the encapsulation process discussed previously. The bottom interconnect layer (buried feedthrough) is used to deliver electrical signals into and out of the micropackages while avoiding contact with the Al-based package anchor. The top interconnect is used to construct the RF microstructures (CPW's) as well as the pads that are used to deliver electrical signals to or from outside instruments or circuitry. More details about the specific design (layout) and functionality of the RF microstructures are discussed in Chapter 5.

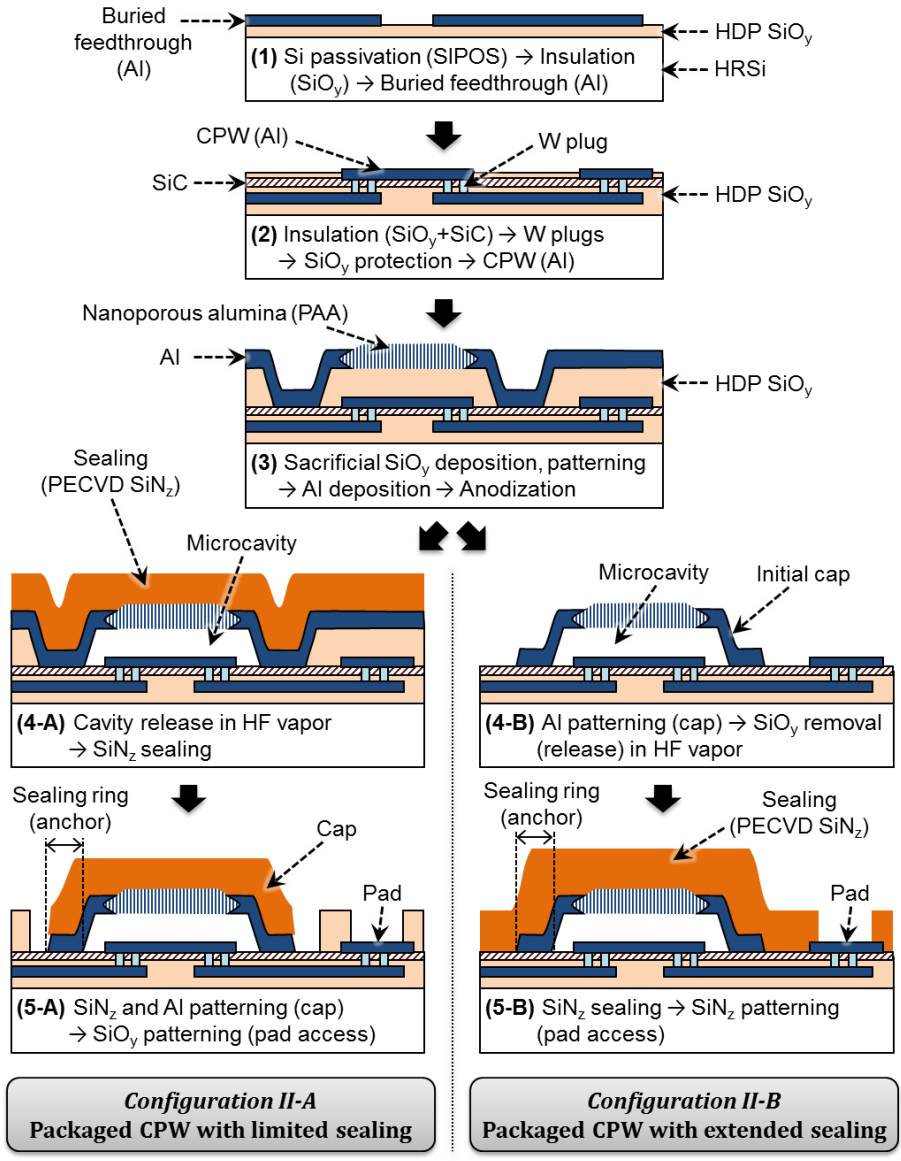


Fig. 2.16 Cross-sectional schematics illustrating two process flows (based on 8 masks) to produce wafer-level packaged RF transmission lines (CPW's). *Configuration II-A* involves packages with limited lateral extension of the sealing layer, whereas *Configuration II-B* involves packages with a laterally extended sealing layer.

The substrates used in this process are high resistivity Si (HRSi) wafers of 200 mm diameter, 0.7 mm thickness and nominal resistivity of more than 1500 Ω.cm. First, a surface passivation process is applied to the HRSi wafers by depositing a semi-insulating polycrystalline-silicon (SIPOS) layer of 75 nm thickness. This is done by means of a low pressure chemical vapor deposition process (LPCVD). The SIPOS passivation layer is intended to reduce the density of the fixed charges normally present at the silicon-oxide interface, thus suppressing the formation of a conductive channel of mobile charges within the Si that would otherwise increase the RF signal losses (Detcheverry *et al.*, 2004).

After passivating the Si wafer surface, an insulating layer of silicon oxide (SiO_y) of 1 µm thickness is deposited by means of a high density plasma chemical vapor deposition (HDP-CVD) process. Next, the bottom interconnects (buried feedthroughs) are formed by sputter-deposition of an Al-based 0.9 µm-thick metal stack which is then patterned by dry etching (situation **(1)** in Fig. 2.16). This metal stack is next covered by an insulating HDP SiO_y layer which is later planarized by means of chemical mechanical polishing (CMP) down to a thickness of approximately 0.6 µm on top of the buried feedthrough layer. A 0.4 µm-thick silicon carbide (SiC) layer is then deposited to serve as an etch-barrier protecting the underlying silicon oxide against the HF vapor release step later in the process flow

In order to provide electrical connection between the buried feedthrough and the next metal level, 0.4 µm-wide vias are etched in the SiC + SiO_y stack (on top of the buried feedthrough). Next, a thin TiN barrier layer (10 nm) is sputter-deposited and then the vias are filled with tungsten (W) by means of a CVD process. This is followed by a CMP step to remove the excessive W and TiN on top of the SiC layer. Next, a thin SiO_y layer is deposited and patterned on top of the SiC layer to protect it from the following metal etching process. The second metal level which is mainly intended to construct coplanar waveguides (CPW's) is then formed by sputter deposition of a 0.7 µm-thick Al-based metal stack which is patterned by dry etching (situation **(2)** in Fig. 2.16).

After constructing the metal interconnects, a 3 µm-thick silicon oxide sacrificial layer is deposited by means of an HDP-CVD process carried out at 400 °C. This sacrificial SiO_y layer is then patterned by a specially developed dry etching process to create slightly inclined sidewalls as shown in Fig. 2.17. The inclined sidewalls are needed to ensure good edge coverage of the 1.5 µm-thick Al layer which is subsequently deposited on the wafers using a sputtering process at room temperature. Next, masked anodization of the Al

layer results in the formation of 2.3 μm-thick nanoporous alumina membranes (situation **(3)** in Fig. 2.16).

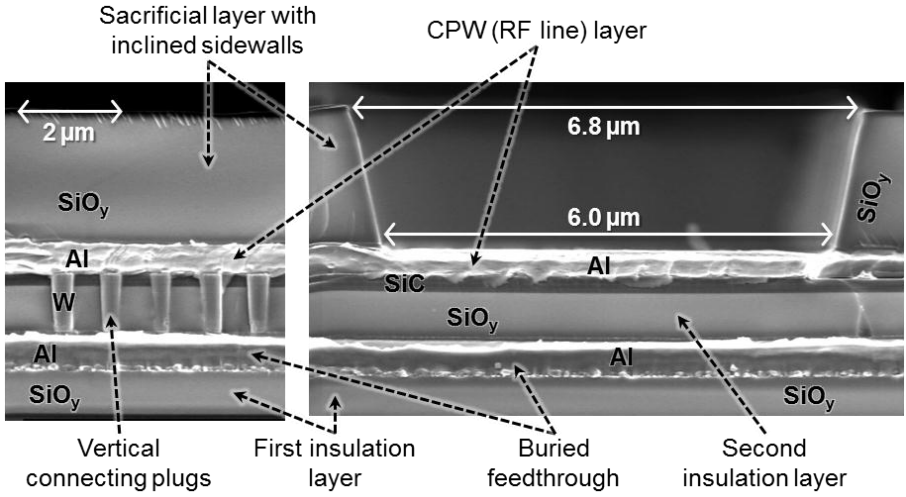


Fig. 2.17 Cross-sectional SEM views of the implemented 2-level metal interconnects and the silicon oxide sacrificial layer with inclined sidewalls.

The subsequent steps of the encapsulation process are implemented in two different routes. In the first route (*Configuration II-A*), the silicon oxide underneath each PAA membrane is etched using HF vapor, and then the microcavities are sealed by depositing a 4 μm-thick PECVD silicon nitride (SiN_z) layer (situation **(4-A)** in Fig. 2.16). Next, the SiN_z and the Al layers are patterned using the same mask to define the package edge, and then the sacrificial oxide layer is patterned using a different mask to access the electrical connection pads (situation **(5-A)** in Fig. 2.16).

The result of this interconnects and encapsulation process flow is a large number of micropackages and other microstructures fabricated by batch processing directly on 200 mm Si wafers as shown in Fig. 2.18. According to the specific process flow of *Configuration II-A* in Fig. 2.16, micropackages are constructed with a cap of approximately 6 μm thickness and a nearly aligned edge of the nitride sealing layer and the Al layer at the package anchor (sealing ring) which is typically 20 μm in width as shown in Fig. 2.19.

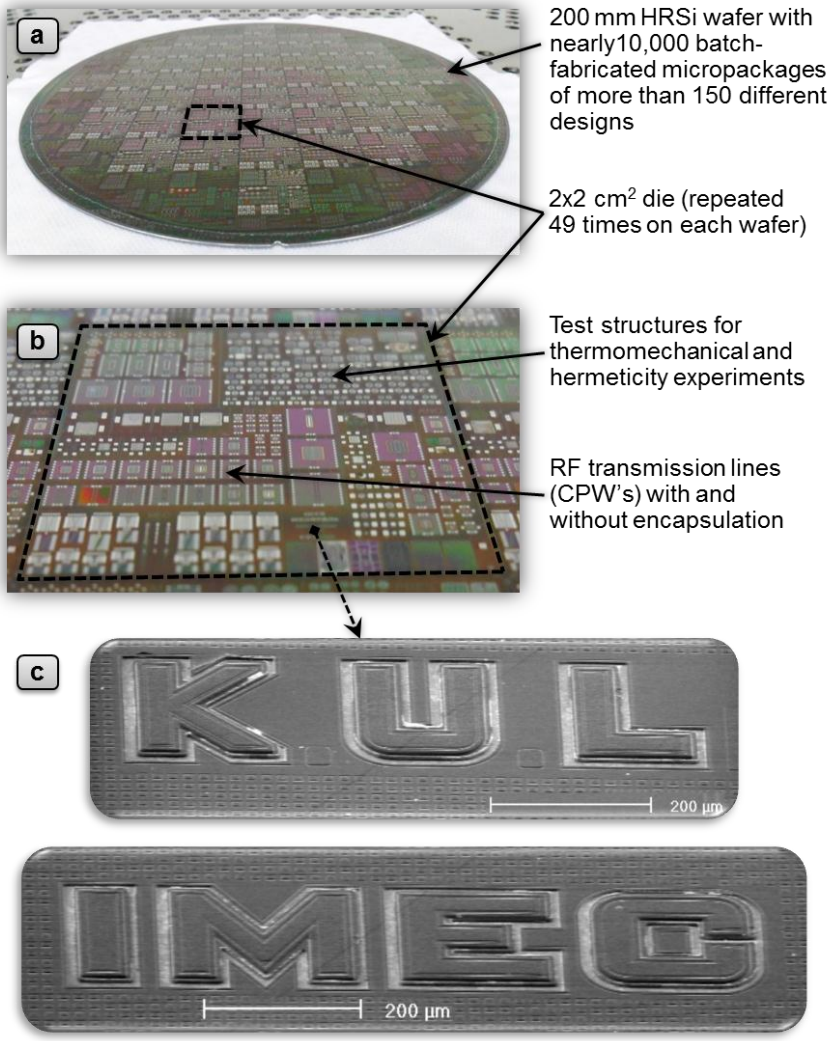


Fig. 2.18 (a,b) Photographs of a 200 mm HRSi wafer after completing the packaged RF lines process flow according to *Configuration II-A* of Fig. 2.16; and (c) SEM of on-wafer micropackages (with sealed microcavities) shaped as the letters of KU Leuven and imec logos.

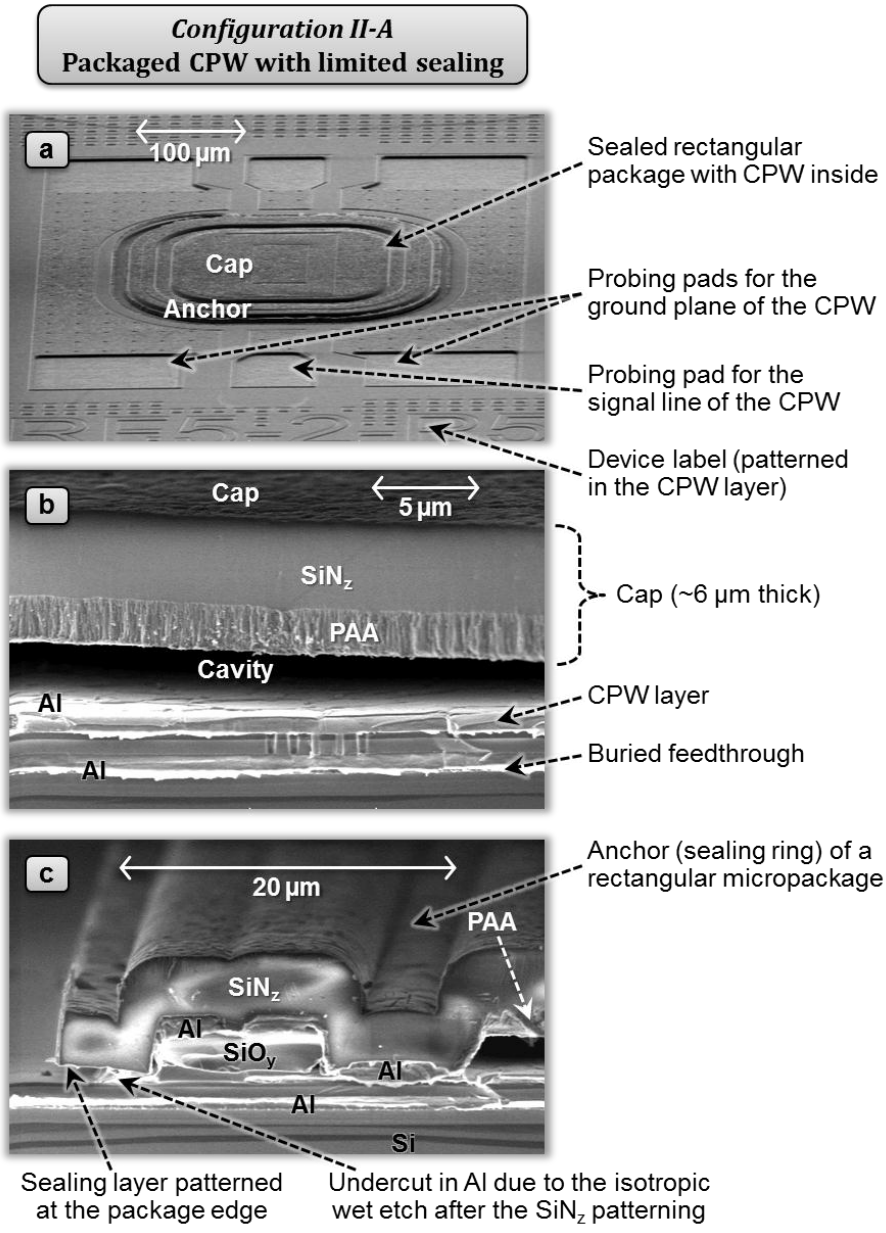


Fig. 2.19 Tilted and cross-sectional SEM views of on-wafer packaged RF lines (CPW's) with limited lateral extension of the 4 µm-thick silicon nitride sealing layer, according to *Configuration II-A* of Fig. 2.16.

In an alternative route for completing the packaging process (according to *Configuration II-B* in Fig. 2.16), the Al capping layer is patterned directly after the anodization process. This is followed by removing the sacrificial oxide layer from the entire wafer surface (above the SiC layer) using HF vapor (situation **(4-B)**). Finally, a 6 µm-thick PECVD SiN_z sealing layer is deposited and patterned to provide access to the electrical connection pads (situation **(5-B)**). The resulting micropackages of this encapsulation scheme are shown in Fig. 2.20. A distinctive feature of *Configuration II-B* is the lateral extension of the sealing layer beyond the cap edge (or anchor) as shown in Fig. 2.20(c).

The main differences between the packaging schemes of *Configuration II-A* and *Configuration II-B* are outlined in Table 2.1. Essentially, the lateral extension of the SiN_z sealing layer beyond the cap edge in *Configuration II-B* is expected to enhance the package resistance to gas leakages (as compared to *Configuration II-A*) by covering the exposed thin film interfaces around the Al layer at the package anchor (compare Fig. 2.19(c) and Fig. 2.20(c)). This effect is further investigated in Chapter 4. Furthermore, the use of a thicker sealing layer in *Configuration II-B* is advantageous in terms of the mechanical strength of the micropackages. A number of critical steps are involved in each scheme which can be a source of physical damage to the micropackages. This includes the cap patterning step for *Configuration II-A* and the pad patterning step for both configurations (the stresses caused by the photolithography and etching processes can damage the micropackages). Moreover, the exposed Al edge of the cap (or anchor) during the sacrificial layer etching (release) process for *Configuration II-B* can be a source of damage if the HF vapor used in this process attacks the interface between the Al and the SiC layers.

Table 2.1 A comparison between the wafer-level encapsulation schemes of *Configurations II-A* and *II-B (as shown in Fig. 2.16)*.

	Configuration II-A	***Configuration II-B***
Hermeticity	**Lower** (4 µm sealing layer and exposed interfaces at the cap edge)	**Higher** (6 µm sealing layer, laterally extended to cover the cap edge)
Mechanical strength	**Lower** (4 µm sealing layer)	**Higher** (6 µm sealing layer)
Critical processing steps	• Cap patterning is performed on top of the micropackages. • Pad patterning is performed on top of the micropackages.	• Cap edge is exposed during the sacrificial layer etching (Al to SiC adhesion can be compromised). • Pad patterning is performed on top of the micropackages.

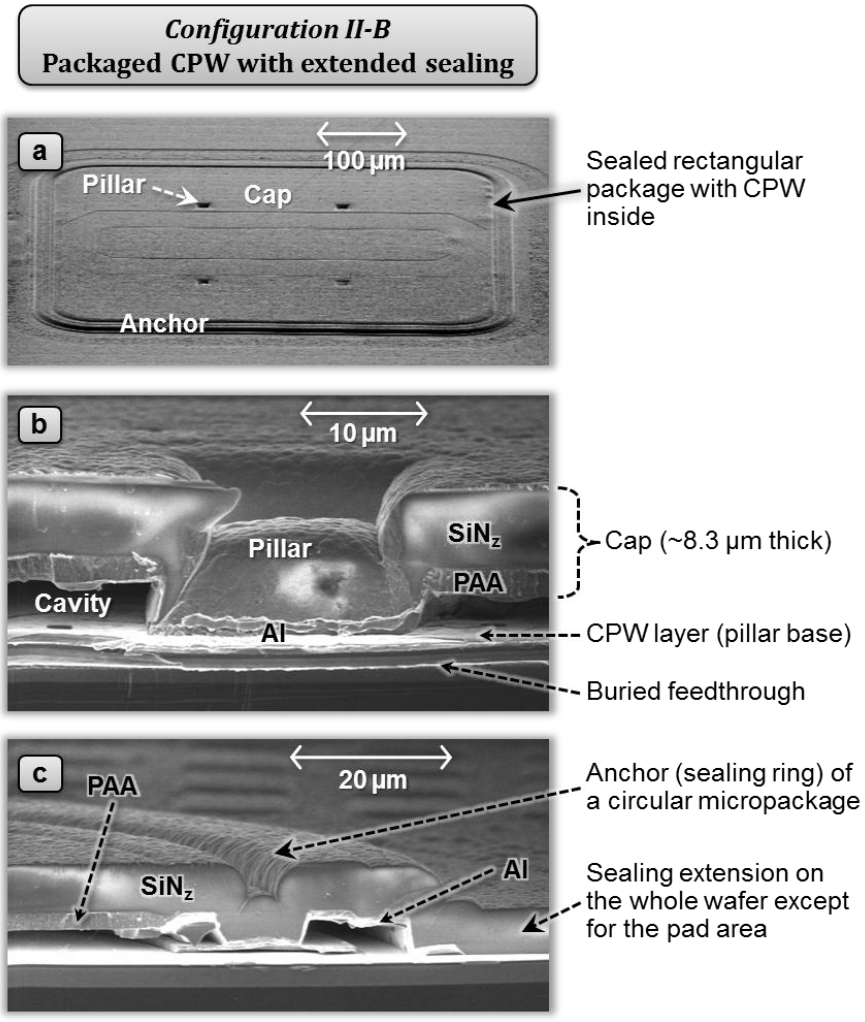


Fig. 2.20 SEM views of on-wafer packaged RF lines (CPW's) with laterally extended 6 µm-thick silicon nitride sealing layer, according to *Configuration II-B* of Fig. 2.16.

2.7 Wafer-level encapsulation of Ni-based MEMS

A further step has been taken in the direction of integrating the new encapsulation technique with advanced microsystems. Namely, a complex integration experiment is launched to study the compatibility of the packaging

process based on nanoporous alumina with Ni-based MEMS. In the following subsections, the main findings of this integration experiment are discussed.

2.7.1 Nickel as a structural material for MEMS

Electroplated nickel has been under investigation over the past two decades as a viable alternative for the more traditional microsystems materials like silicon and its compounds (Spearing, 2000). Micromirrors for optical systems (Akimoto *et al.*, 1997), micromechanical switches for power and RF systems (Zavracky *et al.*, 1997; Majumder *et al.*, 2003; Ekkels, 2011), miniature power generators (Fang *et al.*, 2006) as well as microresonators (Huang *et al.*, 2008) are all examples of MEMS realized using electroplated Ni. The most attractive properties of nickel and its alloys in this regard include their low-temperature deposition process (electroplating), high electrical conductivity, ferromagnetic properties, high mass density, high elastic modulus, high hardness, relative chemical stability and resistance to corrosion (Myung *et al.*, 2003; Ekkels, 2010).

Controlling the internal stress and its distribution within Ni thin films in a reproducible fashion has usually been a challenge as reported by Tsuchiya (2008) and Ekkels (2010). This challenge is in fact rather common in surface micromachining processes, irrespective of the materials used (Spearing, 2000). The overall internal stress and its distribution in a Ni layer are particularly sensitive to high temperature exposures as indicated by the experimental results shown in Fig. 2.21(a). In this experiment, Ni microstructures of approximately 2.3 μm thickness are created on top of a SiO_y sacrificial layer by means of an electroplating process in a sulphamate bath at 55 °C using a fixed current density of 0.5 A/dm^2. A thin seed layer needed for the electroplating process is typically present underneath the Ni microstructures (composed of 30 nm TiW and 150 nm Cu). After the electroplating process, different samples with Ni microstructures are annealed at different temperatures in the range of 200 to 400 °C for approximately one hour. Next, all samples are subjected to a release process (sacrificial SiO_y layer removal) in HF vapor in order to obtain freestanding Ni microstructures.

The average in-plane stress of the Ni structures is obtained using a micromechanical strain gauge, based on a concept proposed by Lin *et al.* (1997). This strain gauge is essentially made of a relatively long Ni test beam which is fixed at one end and connected at the other end through a short horizontal (slope) beam to a rotating (indicator) beam. This indicator beam translates the strain (elongation or shrinkage) of the Ni test beam into a

certain rotation or displacement (δ_h) that can be visually read out on a micro-Vernier scale using a microscope (see Fig. 2.21(b)). Using an approximate linear model developed by Lin *et al.* (1997), the in-plane Ni stress (σ) can be expressed as a function of the horizontal displacement at the Vernier scale (δ_h) as follows:

$$\sigma = \frac{2\,E\,l_{sb}\,\delta_h}{3\,l_{ib}\,l_{tb}\,F}\;; \quad F = \frac{1-(w_{ib}/l_{sb})^2}{1-(w_{ib}/l_{sb})^3} \tag{2.4}$$

where E is the elastic modulus of electroplated Ni (around 150 GPa), l_{sb} is the length of the slope beam (20 μm), l_{ib} is the length of the indicator beam (200 μm), l_{tb} is the length of the test beam (500 μm) and w_{ib} is the width of the indicator beam (4 μm). In this case, equation (2.4) yields a stress sensitivity of 20 MPa per micrometer of displacement at the Vernier scale (which is designed to reveal displacements with a resolution of 0.5 μm).

The distribution of the in-plane stress within the Ni layer is in most cases not uniform (*i.e.*, the value of the stress at the bottom of the layer is different from that at the top of the layer). This can be translated into a linear out-of-plane strain gradient (Γ, or the strain change per unit thickness of the layer) which is in turn related to the vertical deflection (δ_v) of a cantilever beam (as in Fig. 2.21(c)) by the equation: $\Gamma = 2\,\delta_v\,/\,{l_c}^2$ (Ekkels, 2010); where l_c is the length of the cantilever (different lengths in the range of 100 to 500 μm are employed as shown in Fig. 2.21(c)).

The results in Fig. 2.21(a) show an increasing tensile stress of the Ni layer at higher annealing temperatures—starting with a low compressive (negative) stress in the layer when released without anneal (as-deposited at 55 °C). The increasing tensile stress is mainly attributed to a recovery, recrystallization and grain-growth mechanism as explained by Buchheit *et al.* (2002). In simple terms, the Ni atoms are being rearranged by the annealing process, causing tension (or shrinkage) as the rearranged atoms occupy less space compared to their initially random distribution. Furthermore, changes in the out-of-plane strain gradient also take place after annealing due to the varying boundary conditions between the upper and lower surfaces of the Ni layer. While the upper surface of Ni is free to shrink during the annealing process, the lower surface is fixed to the underlying seed layer and sacrificial layer. The result is more shrinkage or tension in the upper surface compared to the lower surface which causes the increasing out-of-plane strain gradient as observed in Fig. 2.21(a). Despite the relatively high values of the in-plane stress and out-of-plane strain gradient after exposure to 400 °C (which is the deposition temperature of the sacrificial HDP-CVD silicon oxide), functional

MEMS devices can be obtained if properly designed to mitigate the impact of such high stress and gradient levels. Good adhesion at the anchor points of the MEMS structures is also important in this case in order to withstand the pulling force caused by the tensile stress.

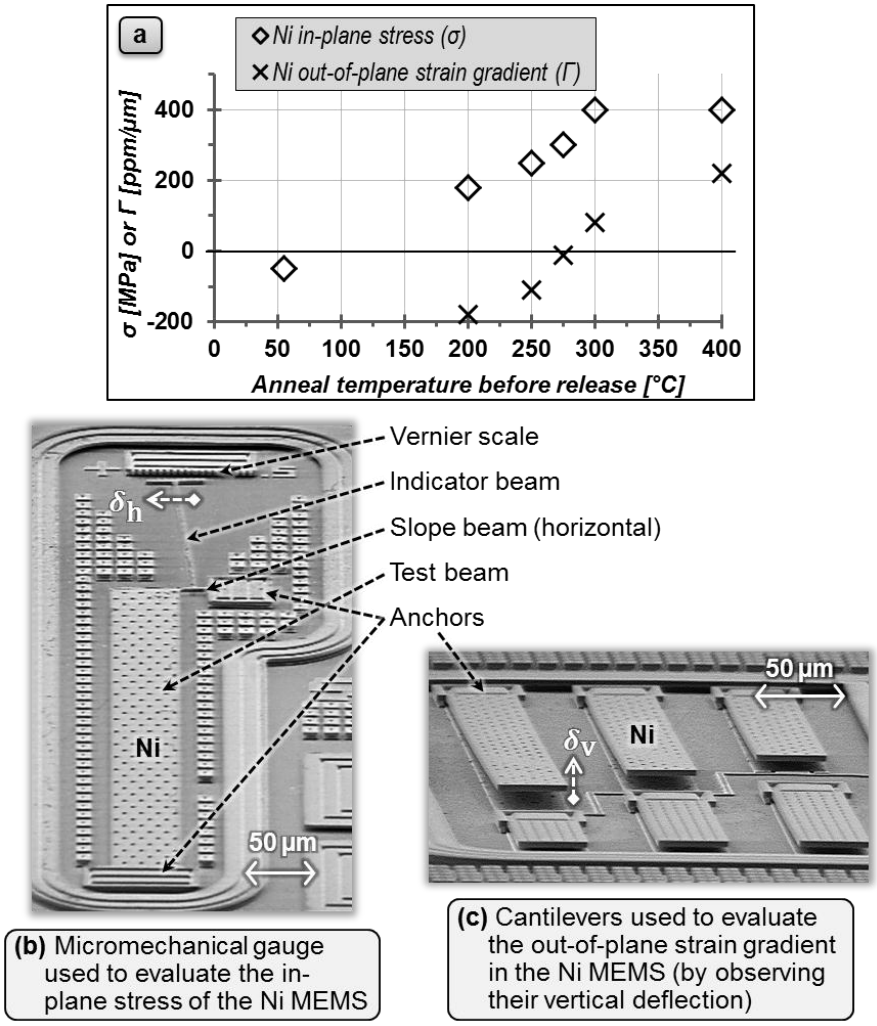


Fig. 2.21 (a) The average in-plane stress and the out-of-plane strain gradient of 2.3 μm-thick electroplated Ni microstructures annealed at different temperatures and then released in HF vapor. Positive values correspond to a tensile in-plane stress and an upward increase in the tensile strain (upward deflection of cantilevers). (b,c) SEM views of the Ni microstructures used to obtain the results in (a).

2.7.2 Fabrication and encapsulation of Ni-MEMS

Wafer-level encapsulated Ni-MEMS devices have been realized in order to examine the challenges of integrating the PAA-based encapsulation process with an advanced MEMS technology. This integration is further intended to facilitate precise monitoring of the internal pressure of the micropackages by means of embedded pressure-sensing devices as discussed in Chapter 4. The process flow shown in Fig. 2.22 illustrates the main stages involved in fabricating and encapsulating the Ni-based microsystems.

The fabrication process begins as previously discussed in section 2.6 by passivating the surface of the 200 mm HRSi wafers using a thin SIPOS layer. This is followed by a number of deposition, patterning and planarization steps to form two levels of Al-based interconnects (situation **(1)** in Fig. 2.22, similar to situation **(2)** in Fig. 2.16). Next, a first level of the sacrificial layer (HDP SiO_y) is deposited and planarized using CMP (final SiO_y thickness above the Al layer is 2 µm). Small recesses of 100 or 200 nm depth are then introduced in the sacrificial layer using a dry etching process in order to create vertical stoppers for the MEMS devices as shown in Fig. 2.22. The formation of the MEMS structures then begins by depositing a seed layer composed of 30 nm TiW and 150 nm Cu. This is followed by the formation of a 5 µm-thick photoresist mold in order to define the shape of the Ni microstructures. Next, a Ni layer of approximately 2.3 µm thickness is grown into the photoresist mold using an electroplating process in a sulphamate bath at 55 °C with a current density close to 0.5 A/dm^2.

The resulting Ni layer and the underlying Al-based interconnects are shown in Fig. 2.23. The photoresist mold and the underlying seed layer are then removed by means of selective wet etching in a standard solvent, followed by a commercial Cu etching solution and then a TiW etching solution based on hydrogen peroxide (situation **(2)** in Fig. 2.22). At this stage in the process flow, wafers with Ni-MEMS devices can be released using an HF vapor etching process in order to verify the operation and the characteristics of the Ni microstructures. Examples of Ni-MEMS structures before encapsulation are shown in Fig. 2.21 and Fig. 2.24.

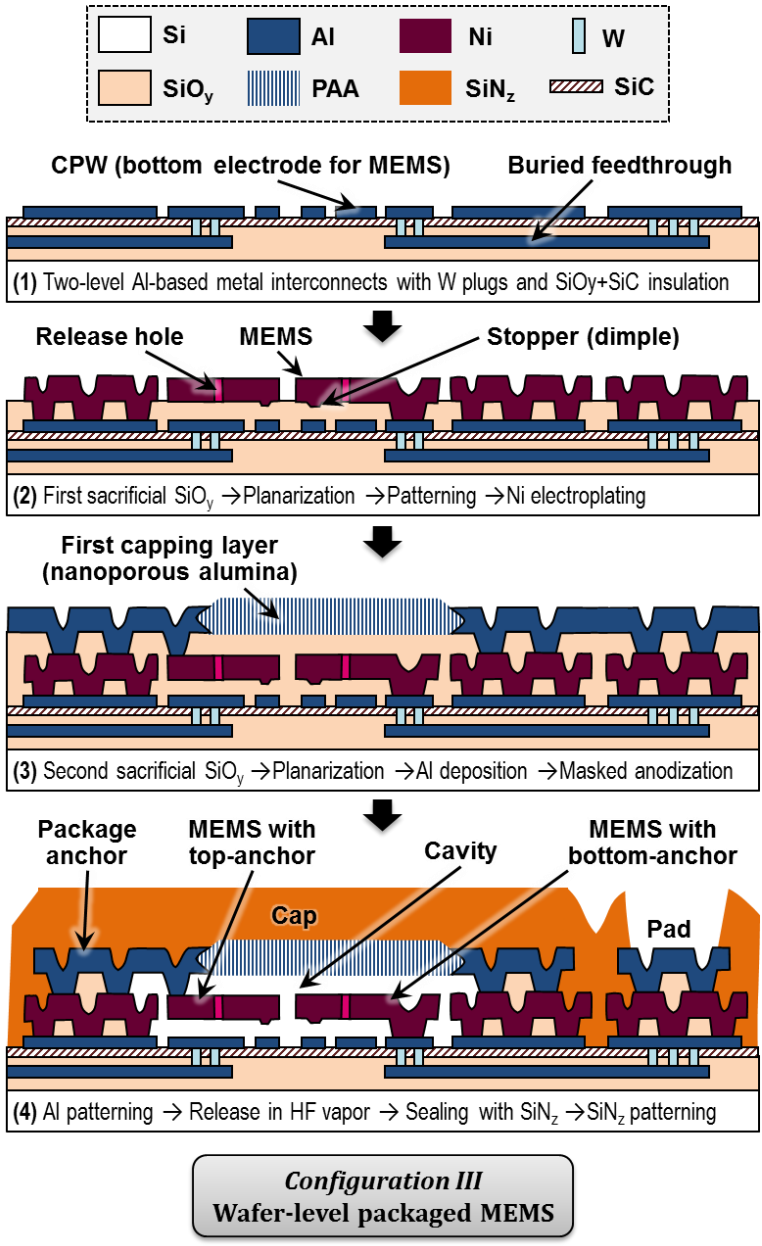


Fig. 2.22 Cross-sectional schematics illustrating the surface micromachining process flow (based on 11 masks in total) for the fabrication of wafer-level packaged MEMS. A wide range of encapsulated MEMS and microstructures can be realized using this process flow.

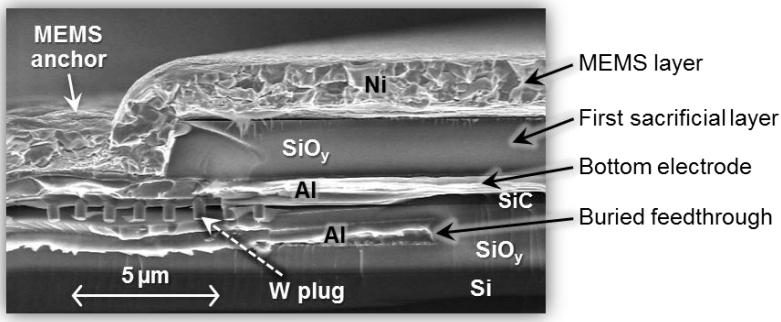


Fig. 2.23 Cross-sectional SEM view of the Al-based interconnects and the Ni MEMS layer on a 200 mm Si wafer.

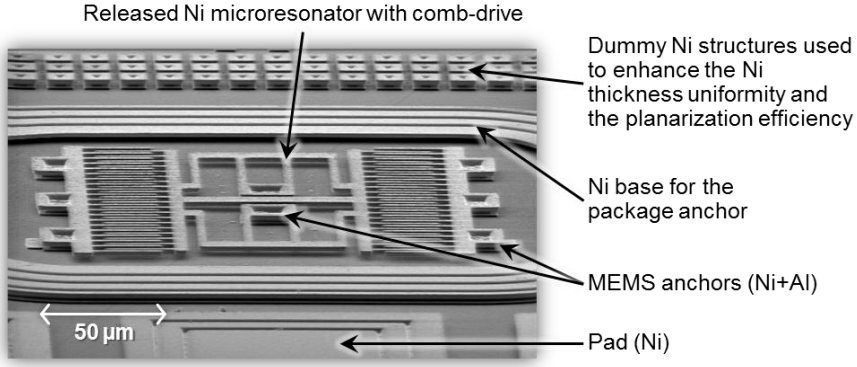


Fig. 2.24 SEM view of a released Ni microresonator before applying the wafer-level encapsulation process.

The wafer-level MEMS encapsulation process begins with the deposition of a second sacrificial layer (2 µm-thick) on top of the MEMS structures. The choice of the material and the deposition process for this second sacrificial layer was found to be critical in this scheme due to the sensitivity of the Ni layer to high temperature exposure as discussed earlier. HDP SiO_y which is deposited at 400 °C induces a high tensile stress and strain gradient in the Ni, but it is generally preferred—and therefore chosen here—as a sacrificial layer due to its high mechanical and chemical stability. Alternatively, a polymer deposited at a low temperature can be used as a sacrificial layer to avoid the high temperature impact on the Ni layer. However, polymers (like photoresists) present additional challenges because of their sensitivity to various chemical processes and to temperature variations. Moreover, polymers are a potential source of organic residues which are known to cause substantial outgassing inside sealed microcavities (Sarvar *et al.*, 2002).

To create the cap, the second sacrificial layer (SiO_y) is patterned to create anchoring points for the cap on top of the Ni layer. This is followed by the deposition and localized anodization of a 2 µm-thick Al layer (situation **(3)** in Fig. 2.22). The Al layer is then patterned to define the edges of the micropackages as well as the electrical connection pads. This is followed by removing all the sacrificial silicon oxide (inside and outside the microcavities) by means of an HF vapor etch process for a duration close to 4 hours. The long duration of the release process is caused by the relatively slow etch rate used to avoid any damage to the PAA membranes from excessive water generation as previously discussed in section 2.4. Moreover, removing the sacrificial oxide layer underneath the MEMS structures is time consuming because the etch process has to laterally extend between the release holes present in the MEMS structures which are typically 10 µm apart. At this stage the released MEMS structures are encapsulated by nanoporous alumina membranes as shown in Fig. 2.25. The effect of the high tensile stress in the Ni layer can be seen in the local damage to the SiC layer around the edges of the probing pads as shown in Fig. 2.25(a). Another cause for this damage to the SiC layer is the relatively low selectivity of the dry etching process used to pattern the Al interconnects below the Ni structures (CPW layer in Fig. 2.22).

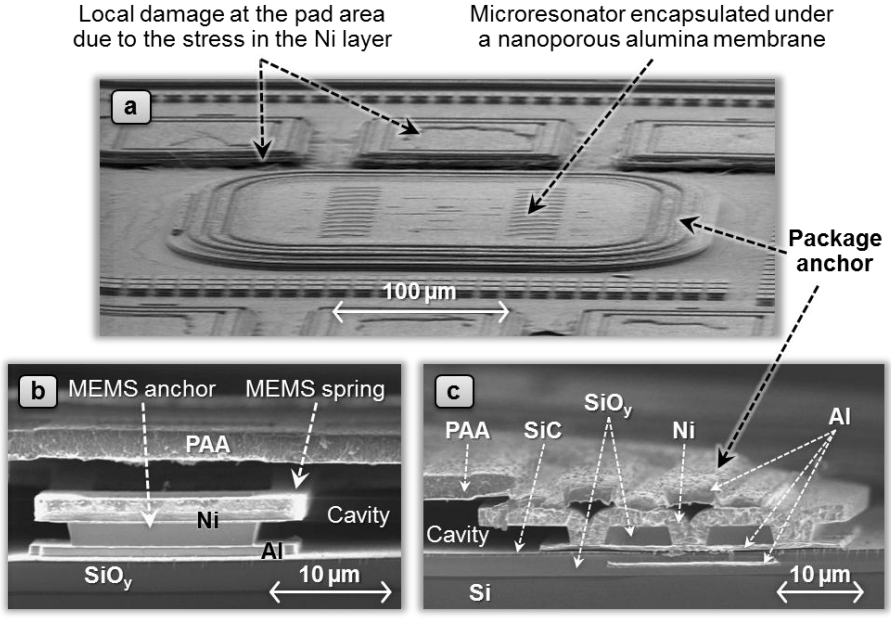


Fig. 2.25 SEM views of a released microresonator (as in Fig. 2.24) encapsulated underneath a nanoporous alumina membrane.

The microcavities formed around the MEMS structures using nanoporous alumina membranes are sealed by depositing an impermeable material such as silicon nitride, yielding on-wafer encapsulated MEMS as shown in Fig. 2.26. The SiN_z sealing layer used in this case is 4 μm in thickness and is deposited by means of a PECVD process performed at a pressure of 0.01 mbar and a temperature of 250 °C. What remains in order to complete this process flow is to pattern the nitride sealing layer in order to provide access to the probing pads which are used for electrical contact with the encapsulated devices (situation **(4)** in Fig. 2.22). Unfortunately this last step was not successfully performed because of the delamination of a number of layers and microstructures on the wafers. This can be seen in the physical damage observed at the pad area in Fig. 2.25(a), as well as the damage to relatively large packages shown in Fig. 2.26(a). These delaminations are believed to be caused by the high tensile stress in the Ni structures, the damage to the SiC layer, as well as the residual (tensile) stress in the sealing nitride layer used in this specific process flow.

Being able to perform the last nitride patterning step and electrically test the encapsulated Ni-MEMS would be possible by adjusting the processing scheme as follows:

- Reducing the Ni stress (by using a sacrificial layer deposited at a lower temperature);
- Minimizing the amount of Ni present at the pad area (design change) to suppress the local impact of this stress;
- Protecting the SiC layer from the dry etching process of the bottom electrode (or optimizing the etching process); and/or
- Reducing the residual stress in the sealing layer (by optimizing the SiN_z deposition process).

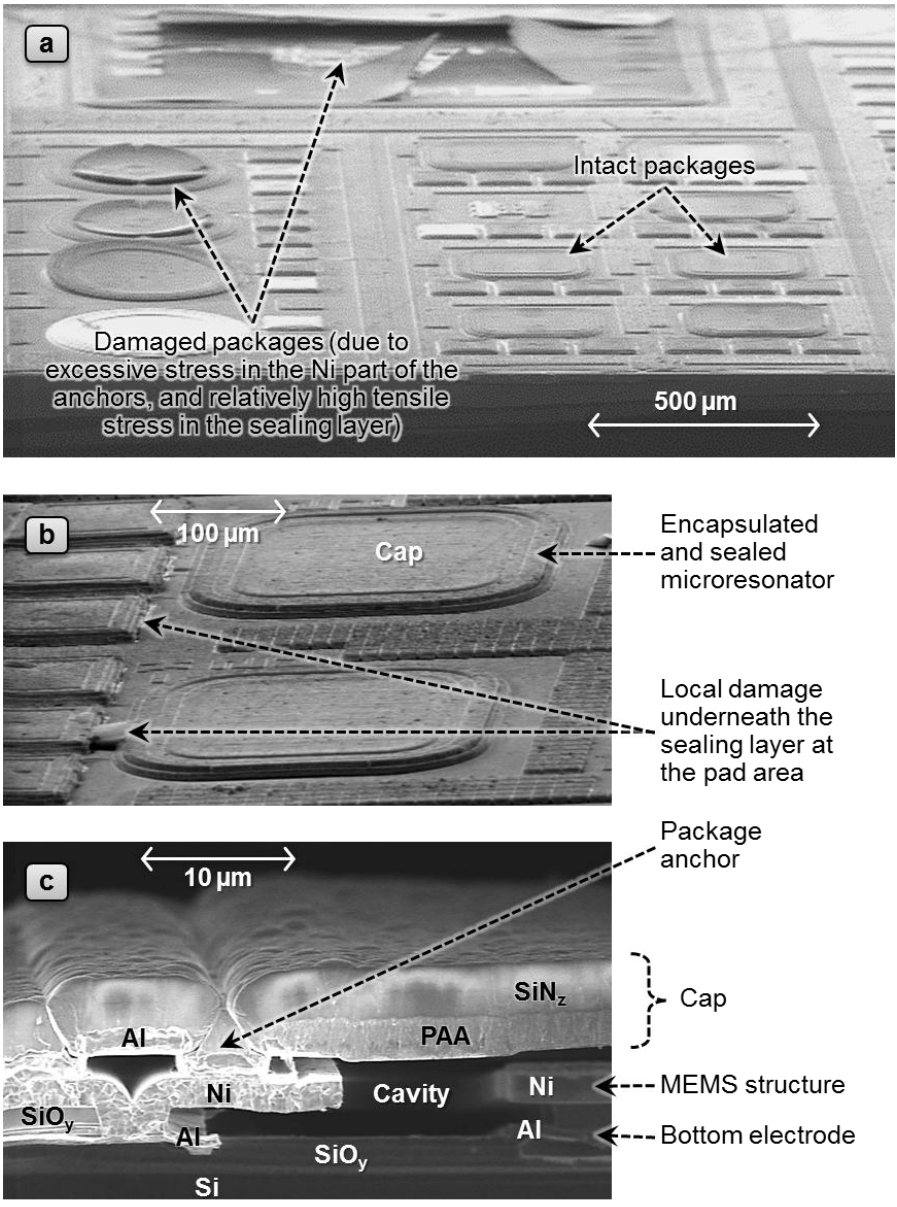


Fig. 2.26 (a) SEM view of a number of micropackages (encapsulating Ni-MEMS) showing the partial damage after the sealing layer deposition; and (b,c) SEM views of a Ni microresonator (as in Fig. 2.24) which is encapsulated using a 3 µm-thick PAA membrane and a 4 µm-thick SiN_z sealing layer.

2.8 Conclusions

The basic processing scheme for wafer-level encapsulation of microsystems using nanoporous alumina employs a novel localized anodization process of Al thin films (1–2 μm thick). The resulting nanoporous alumina membranes feature a high density of cylindrical nanopores which are typically 10 to 20 nm in diameter. By choosing the appropriate electrolyte, potential, temperature and duration of the anodization process, *in situ* removal of the thin AlO_x barrier layer at the bottom of the nanopores is achieved. Neither a hard mask nor seed layers are needed thanks to the novel design of the photoresist mask that significantly improves the stability and reproducibility of the anodization process. Furthermore, silicon oxide and polymer (photoresist) sacrificial layers are successfully etched through the nanoporous membranes producing residue-free microcavities. Sealing of the empty microcavities under low pressure has been achieved by depositing Al (2.6 μm thick) or PECVD silicon nitride (4 to 6 μm in thickness). Moreover, the nitride-sealed thin film packages are optically transparent, promising to facilitate optical inspection and/or operation of the encapsulated microsystems.

A seamless integration of two different configurations of the new micropackages with planar Al-based interconnects (RF transmission lines) is achieved. Furthermore, a rather complex experiment to integrate both Al-based interconnects and the micropackages with Ni-based MEMS indicates a basic compatibility between these three technologies. However, the sensitivity of electroplated Ni structures to high-temperature exposure and other contamination challenges hindered the completion of this integration flow (no electrical tests on encapsulated MEMS devices could be performed).

"Everything must be made as simple as possible, but not one bit simpler."

Albert Einstein (1879–1955)

Chapter 3 Thermomechanical analysis

In this chapter we start with describing analytical and finite element models that are developed to study the thermomechanical behavior of thin film packages based on nanoporous alumina. This is followed by a simulation-based analysis covering the mechanical strength and the impact of temperature variations and residual stresses on the micropackages. Finally, an experimental investigation of the impact of epoxy overmolding (performed at a high pressure and temperature) on the thin film packages is discussed.

3.1 Introduction

The relative novelty and the apparent fragility of thin film packages raise a number of questions regarding their strength and reliability, hence the need for a detailed structural and thermomechanical analysis. Moreover, the use of nanoporous alumina membranes in the package construction adds another complexity due to the anisotropic structure of this material (as shown in Fig. 1.8, Fig. 2.12(c) and Fig. 3.1(a)). The main direction-dependent mechanical properties of this layer should therefore be determined in order to correctly model the behavior of the micropackages. On the one hand, the use of analytical models to capture the global mechanical behavior of the micropackages is efficient in devising basic guidelines for the structural design. On the other hand, a detailed finite element model would be more suitable for studying the impact of certain (3D) geometrical details as well as the complex impact of thermal mismatch among the different materials of the

composite micropackages. Finally, comparing the simulated performance based on analytical and finite element models to the actual performance of the fabricated micropackages is an important step forward in the process of understanding and validating the characteristics of the new micropackages.

3.2 Thermomechanical modeling of the thin film packages

3.2.1 Anisotropic properties of nanoporous alumina

As discussed earlier, the anodization of Al thin films in a low-*pH* solution results in the formation of an alumina layer featuring a high density of cylindrical nanopores arranged in a hexagonal layout. A 3D schematic view of such thin film with hexagonally arranged pores (or holes) is shown in Fig. 3.1(a). This structure of porous anodic alumina (or PAA) displays a large resemblance to a group of materials known as transversely orthotropic materials (Tan, 1994). This kind of materials is characterized by a structure that is fully symmetric in a certain plane called the plane of isotropy (plane "2,3" shown in Fig. 3.1(a,b)). By making use of the symmetry properties of such transversely orthotropic materials, we can describe the elastic deformation of nanoporous alumina using the following form of Hooke's law (Soboyejo, 2002):

$$\begin{bmatrix} \varepsilon_{11} \\ \varepsilon_{22} \\ \gamma_{12} \end{bmatrix} = \begin{bmatrix} 1/E_{11} & -\nu_{21}/E_{22} & 0 \\ -\nu_{12}/E_{11} & 1/E_{22} & 0 \\ 0 & 0 & 1/G_{12} \end{bmatrix} \begin{bmatrix} \sigma_{11} \\ \sigma_{22} \\ \tau_{12} \end{bmatrix} \tag{3.1}$$

The index "1" in equation (3.1) refers to the direction parallel to the length of the pores (*i.e.*, normal to the plane of isotropy), while the index "2" refers to both directions with the plane of isotropy (*i.e.*, $2 = 3$). Equation (3.1) relates the strain tensors (ε, γ) to the stress tensors (σ, τ) by a matrix that describes the orthotropic material properties (compliance matrix). From the compliance matrix in equation (3.1), it can be concluded that the constants that fully describe the elastic deformation of the PAA layer are the out-of-plane and in-plane Young's moduli (E_{11}, E_{22}), Poisson's ratios (ν_{12}, ν_{21}) and the shear modulus (G_{12}). It has further been shown that both Poisson's ratios can be related by the formula (Soboyejo, 2002):

$$\nu_{21} = \nu_{12}(E_{22}/E_{11}) \tag{3.2}$$

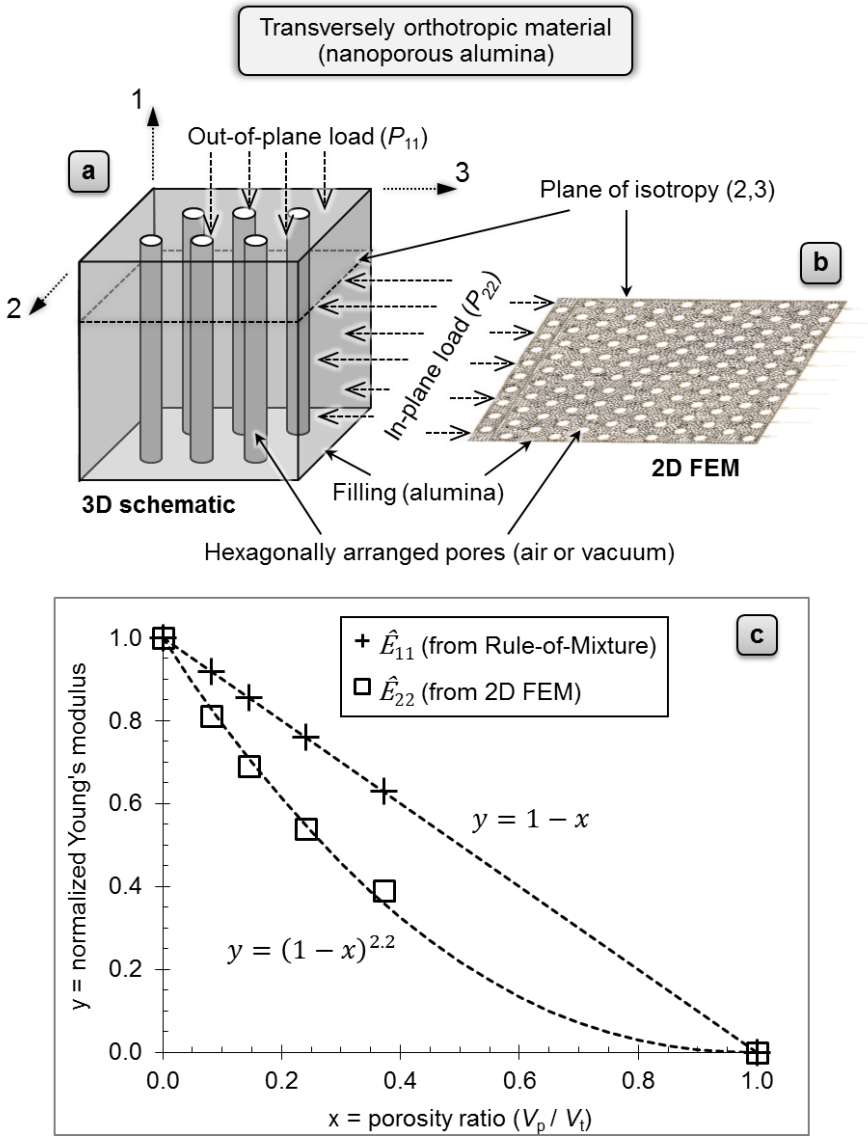


Fig. 3.1 (a,b) A 3D schematic and 2D FEM showing the transversely orthotropic structure of nanoporous alumina; and (c) the normalized out-of-plane Young's modulus ($\hat{E}_{11}$, obtained from the Rule-of-Mixture) and in-plane Young's modulus ($\hat{E}_{22}$, obtained from a 2D FEM simulations) as a function of porosity. $\hat{E}_{11}$ and $\hat{E}_{22}$ are normalized to the Young's modulus value for impermeable anodic alumina (without any pores).

The out-of-plane Young's modulus (E_{11}) can be obtained by applying the Rule-of-Mixture theory in the constant-strain mode (Soboyejo, 2002). Here the material is subjected to an out-of-plane load (P_{11} in Fig. 3.1(a)) which results in the same deformation or strain for both the filling and the pores (hence the term *constant strain*). By observing that the total load can be decomposed into two partial loads applied to the alumina filling and the pores (by their volume or area ratio), the following equation can be written:

$$P_{11} = \sigma_{11} A_t = E_{11} \varepsilon_{11} A_t = E_a \varepsilon_{11} A_a + E_p \varepsilon_{11} A_p \tag{3.3}$$

Where σ_{11} is the out-of-plane stress, ε_{11} is the out-of-plane strain (the same for the alumina filling and the pores), A_t is the total area of the plane of symmetry, E_a is Young's modulus of isotropic alumina (the filling), A_a is the filling cross-sectional area, E_p is Young's modulus of the pores (theoretically equals zero) and A_p is the cross-sectional area of all pores. By removing the zero term of the pores and dividing equation (3.3) by the total area (A_t) and the out-of-plane strain (ε_{11}), E_{11} can be expressed as follows:

$$E_{11} = E_a \frac{A_a}{A_t} = E_a \left(1 - \frac{A_p}{A_t}\right) = E_a \left(1 - \frac{V_p}{V_t}\right) \tag{3.4}$$

From equation (3.4) we obtain the linear relationship shown in Fig. 3.1(c) between the normalized out-of-plane Young's modulus ($\hat{E}_{11} = E_{11}/E_a$) and the porosity of the layer which is defined as the fraction of the cross-sectional area or volume occupied by the pores (A_p/A_t or V_p/V_t).

Furthermore, it is important to accurately calculate the in-plane Young's modulus (E_{22}) since it influences the main deformations in the nanoporous alumina layer in a thin film package. This is attributed to the fact that the cap—and the nanoporous alumina layer—is restricted laterally (in-plane) at its edges but rather free to move vertically (out-of-plane). For many composite materials, E_{22} can be obtained by applying the Rule-of-Mixture mentioned above in the constant-stress mode (by applying an in-plane load (P_{22}) and assuming that the in-plane stress is the same everywhere). By following a similar analysis as before, the following expression can be obtained (Soboyejo, 2002):

$$E_{22\ (\text{const. stress})} = \frac{E_a\, E_p}{V_a\, E_p + V_p\, E_a} \tag{3.5}$$

Given that the theoretical value of E_p is zero (Young's modulus of air), the expression in equation (3.5) also yields a value of zero which is not true for porous alumina. The problem with equation (3.5) is the assumption of a constant stress throughout the whole material. This assumption is in fact

invalid in the case of porous materials because the pores which are essentially made of vacuum or air cannot hold any stress (instead the stress is deviated around their edges). Although more complex analytical (or numerical) models have been developed to describe the in-plane elastic properties of perforated plates (Meijers, 1969), preference has usually been given to empirical and finite element models which yield more accurate results (O'Donnell and Langer, 1962; Rabinovich *et al.*, 1997; Moon, 2004).

A 2D finite element model (representing the plane of isotropy) is therefore used to calculate the equivalent in-plane Young's modulus of porous alumina (see Fig. 3.1(b)). In this model, the porosity of the material is varied while the overall in-plane stress (σ_{22}) and in-plane strain (ε_{22}) are observed under a certain in-plane load (P_{22}, as shown in Fig. 3.1(b)). Typical material properties of impermeable anodic alumina ($E_a = 120$ GPa and $\nu_a = 0.25$) are used to construct the porous material in this model. The variation of E_{22} with porosity according to the finite element simulations are then fitted to a typical empirical power function (Moon, 2004), yielding the following relationship (as in Fig. 3.1(c)):

$$E_{22} = E_a \left(1 - \frac{V_p}{V_t}\right)^{2.2} \tag{3.6}$$

Finally, Poisson's ratios (ν_{12}, ν_{21}) can be estimated to have a typical average value of 0.3 (while preserving the relationship in equation (3.2)). Accuracy in obtaining Poisson's ratio is not essential in the case of thin film packages where no substantial out-of-plane stresses or strains of the porous alumina layer take place. Similarly, shear deformations are less significant than normal in-plane deformations in the porous alumina layer. Therefore, the shear modulus (G_{12}) can be approximated using the formula for linear isotropic materials: $G = E/2(1 + \nu)$ (Gere and Timoshenko, 1997); where E and ν are the average Young's modulus and Poisson's ratio of the porous material. In the following sections of the chapter, the above description of the partially anisotropic properties of nanoporous alumina is employed in different models to investigate the overall thermomechanical behavior of the thin film packages.

3.2.2 Analytical flat plate models for cap deformation

Thanks to the flexibility of thin film technology in defining the lateral shapes of microstructures, a thin film package can be constructed according to different layouts as shown in the in Fig. 3.2(a). One of the common mechanical loads encountered by such micropackages is the pressure difference between

the internal cavity (typically sealed under low pressure) and the surrounding atmosphere or processing pressure. Existing analytical models for flat plates with fixed edges (Young and Budynas, 2002) can be used to estimate the response of the cap to a uniform (differential) pressure load as presented in Table 3.1 and Fig. 3.2.

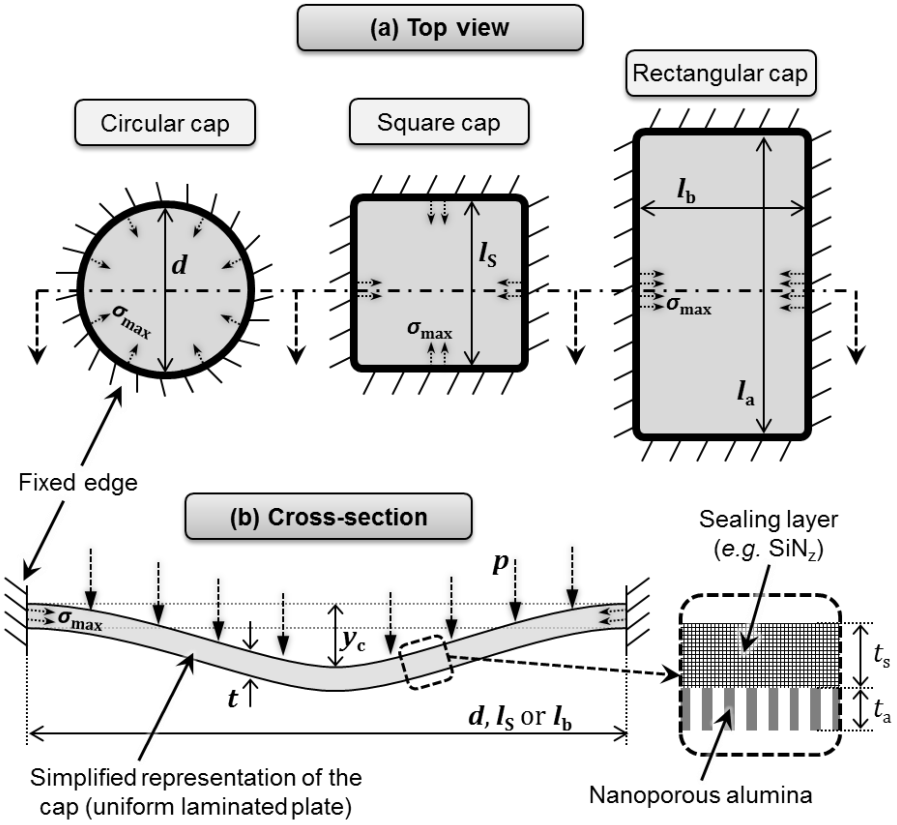


Fig. 3.2 (a) Top-view schematics showing 3 basic cap shapes represented by flat plates with fixed edge; and (d) cross-sectional schematic showing the deformation of any of the 3 thin plates under a uniform load (pressure).

Table 3.1 Analytical formulas (Young and Budynas, 2002) for the center deflection and maximum edge stress in a flat plate with fixed edges under a uniform pressure load (P). The model parameters are visualized in Fig. 3.2.

Plate (cap) shape	Center deflection $\lvert y_c \rvert$	Max stress $\lvert \sigma_{max} \rvert$
Circular	$0.0107\ Pd^4/Et^3$	$0.1875\ Pd^2/t^2$
Square	$0.0138\ Pl_S{}^4/Et^3$	$0.3078\ Pl_S{}^2/t^2$
Rectangular ($l_a > 2l_b$)	$\approx 0.0284\ Pl_b{}^4/Et^3$	$\approx 0.5\ Pl_b{}^2/t^2$

In these simplified models, the Al portion of the cap and the exact geometry of the package edge are not included (compare Fig. 2.1 and Fig. 3.2(b)). Furthermore, Poisson's ratio is assumed to be of a typical value of 0.3 for all materials in order to obtain simple expressions for the deflection and stress. For the equations in Table 3.1: P refers to the pressure difference across the plate, t is the total plate thickness ($= t_a + t_s$), d is the diameter of a circular plate, l_S is the side length of a square plate, and l_b is the shortest side length of a rectangular plate. Assuming the plate is composed of two laminated layers as shown in Fig. 3.2(b), the equivalent Young's modulus of the plate (E) can be estimated as a thickness-weighted average of the in-plane Young's modulus of nanoporous alumina (E_{22}) and Young's modulus of the sealing layer (E_s), according to the formula: $E = (E_{22}t_a + E_s t_s)/t$.

The expressions in Table 3.1 illustrate the impact of the cap size, shape, and thickness on the response to a uniform pressure load. A circular cap undergoes less deformation (y_c) and experiences less maximum stress (σ_{max}) in comparison to a square or a rectangular cap under the same load with the same smallest lateral dimension (*i.e.*, if $d = l_S = l_b$). The same can be stated about a square cap in comparison to a rectangular cap. Moreover, the full symmetry of a circular cap leads to a uniform distribution of the maximum occurring stress (σ_{max}) at the cap edge as shown in Fig. 3.2(a). This is different in the case of a square or rectangular cap where the maximum stress is concentrated at the middle point of the longest edge (see Fig. 3.2(a)). This high stress concentration in the square and rectangular caps is in fact undesired because it increases the probability of damage or fractures under extreme loads.

The analytical flat plate models discussed above provide an elementary and important understanding of the mechanical behavior of thin film packages. However, the formulas in Table 3.1 ignore several thermomechanical and structural details that can be of importance under certain handling and processing conditions of the micropackages. These details include temperature variations, thin film residual stresses, composite layers, 3D geometry details and non-linear effects (*e.g.*, plastic deformations). Therefore, an extensive finite element model (FEM) for a complete micropackage is developed to investigate the detailed thermomechanical behavior of the thin film packages as discussed hereafter.

3.2.3 Finite element model of thin film packages

Based on the previously discussed orthotropic properties of nanoporous alumina, a 2D axisymmetric finite element model (FEM) is created using MSC Marc simulation software (www.mscsoftware.com). A 3D expanded view of this model is shown in Fig. 3.3. The circular package shape is obtained by the axisymmetric boundary condition. As mentioned earlier, a circular package is preferred to other shapes in order to reduce the impact of high external pressure on the cap. As shown in Fig. 3.3, an optional supporting pillar is introduced at the center of the package in order to limit its deformation under high differential pressures as discussed later. Table 3.2 presents the main isotropic material properties used in this model which include: Young's modulus (E), Poisson's ratio (ν), the ultimate stress (σ_u, the limit at which a material starts to yield or fracture), and the coefficient of thermal expansion at room temperature (CTE).

In this model, Al is assumed to deform in a linear elastic manner up to its yield stress limit (0.12 GPa). Beyond this stress value it starts deforming in a pure plastic manner (*i.e.*, constant stress independent of the strain). The expected fracture limit for the elongation strain in thin film Al is reported in the literature to be around 22.5% (Read *et al.*, 2001). The properties of nanoporous alumina are further calculated based on the impermeable anodic alumina properties in Table 3.2 together with the porosity-dependent orthotropic model discussed earlier (see equations (3.4, 3.6) and Fig. 3.1). The layer porosity (V_p/V_t) is mainly dependent on the fabrication process and is considered here to be of a typical value of 24% which is consistent with the experimental results presented earlier in Chapter 2 (a typical pore diameter of 18 nm and an interval of 50 nm between the pores). It is further assumed in this model that both Al and PAA have the same thickness. This is intended to simplify the model geometry. In an actual micropackage the Al layer thickness

is around 33% less than that of PAA due to the volume expansion that takes place in the anodization process.

Various boundary and initial conditions can be applied to this FEM, such as the differential pressure on the cap, the residual stresses in the package layers as well as temperature variations. Furthermore, the model is flexible in assigning geometrical parameters and material properties as a result of using a script-based method for the model construction. In the following section, the simulation results of this FEM (and the previously mentioned flat plate model) are discussed for different packaging structures under different loading conditions.

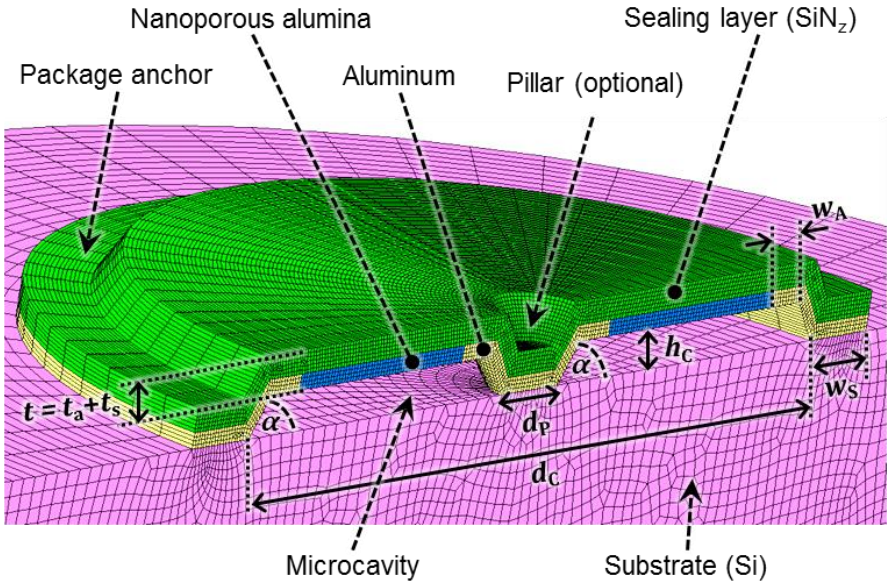


Fig. 3.3 A 3D view of the axisymmetric finite element model of a circular package based on nanoporous alumina. The geometrical parameters of the model are: h_C (cavity height), α (anchor and pillar inclination angle), t_a (alumina layer thickness), t_s (sealing layer thickness), d_C (cavity diameter), d_P (pillar diameter, optional), w_S (width of the anchor edge or sealing ring) and w_A (Al extension inside the cavity).

Table 3.2 Typical mechanical and thermal properties of the materials used in the thin film package model of Fig. 3.3.

	Si substrate (100) in bending mode (Hopcroft *et al*, 2010)	Sputtered Al (Thornton and Hoffman, 1989; Read *et al*, 2001)	Impermeable anodic alumina (Grosskreutz, 1969; Alcala *et al*, 2002)	PECVD SiN_z (Ziebartl *et al*, 1998; Martyniuk *et al*, 2004; Huang *et al*, 2006)
E [GPa]	170	70	120	160
ν	0.064	0.35	0.25	0.25
σ_u [GPa]	5.0 (fracture)	0.12 (yield)	0.18 (fracture)	1.0 (fracture)
CTE [ppm/K]	2.6	23.0	8.1	3.0

3.3 Simulated performance

3.3.1 Structural design and mechanical strength

The structural design of a thin film package is crucial in achieving the required form factor, while at the same time providing sufficient mechanical strength. In a perfectly clamped structure, the aspect ratio of the cap (d/t) essentially determines the overall strength of the micropackage under external (pressure) loads (see Table 3.1). However, in a real micropackage, other geometrical details—such as the presence of a pillar and the inclination angle of the package anchor—can still influence the package performance.

Table 3.3 presents FEM simulation results for 3 different supporting configurations of a package of 4 μm cap thickness (1 μm Al/PAA + 3 μm SiN_z), 350 μm cavity diameter and 5 μm cavity height under 1 bar hydrostatic pressure. In this particular simulation, the cap layers are assumed to be free of any residual stresses at room temperature. The simulation results show that for packages with 60° edge inclination angle, a significant reduction of the cap deformation can be achieved by placing a pillar (of 10 μm diameter in this case) at the center of the package. This however comes at the expense of a higher strain in the Al layer in the introduced pillar structure (0.36% in the introduced pillar compared to 0.13% in the anchor of the package without a pillar). The simulation results further demonstrate a slight enhancement in the mechanical performance (reduced cap deformation and reduced stress

and strain concentrations) by reducing the inclination angle (α) of the anchor and the pillar from 60° to 40°. This is illustrated in Fig. 3.4 and the two rightmost columns of Table 3.3.

The simulation results in Fig. 3.4 also illustrate the advantage of the lateral extension of the Al layer on top of the microcavity (w_A = 5 µm). The elastic (Al) structure at the edge of the membrane absorbs the stress concentration at the corner of the pillar (or anchor) and therefore prevents potential damage to the brittle PAA and SiN_y layers. Such extension of the Al layer at the membrane edge can be easily realized using the masked anodization process described earlier in Chapter 2.

Besides the pressure difference between the internal package environment and the surrounding atmosphere, a micropackage can be subjected to more extreme loads as in the case of an epoxy overmolding process. In this typical 1-level packaging process for IC's, a hydrostatic molding pressure in the range of 25 to 100 bar can be used. To illustrate the impact of such high hydrostatic pressure on a thin film package, simulated results are shown in Fig. 3.5 for circular micropackages featuring an 8.3 µm-thick cap (2.3 µm Al/PAA + 6 µm SiN_y) with 60° inclination angle at the edges, under a differential pressure load of 30 bar at room temperature. The cap layers are assumed to be free of any residual stresses at room temperature.

Table 3.3 Simulated mechanical response of different configurations of a circular micropackage of 4 µm cap thickness and 350 µm cavity diameter (under a differential pressure of 1 bar). The results are obtained using the material properties in Table 3.2 and the FEM shown in Fig. 3.3.

	$\alpha = 60°$ Without pillar	$\alpha = 60°$ With pillar (Fig. 3.4(a))	$\alpha = 40°$ With pillar (Fig. 3.4(b))
Center deflection [µm]	2.3	0.38	0.33
Max total strain in Al [%]	0.13 (in anchor)	0.36 (in pillar)	0.17 (in pillar)
Max principal stress in SiN_y [MPa]	158	165	123
Max principal stress in PAA [MPa]	60	25	24

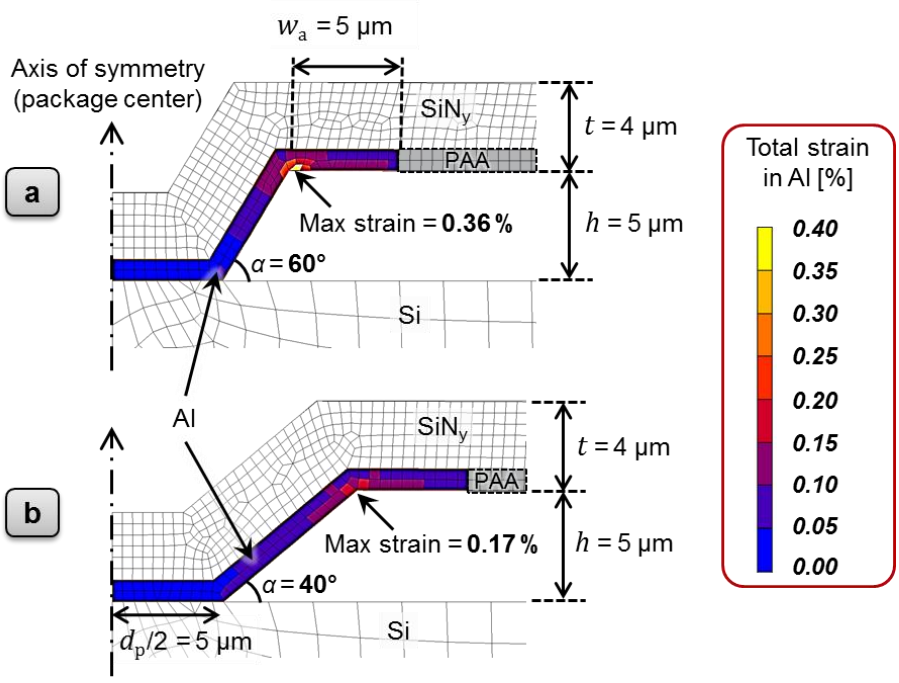


Fig. 3.4 Simulated strain distribution the Al layer for two different pillar geometries of micropackages subjected to 1 bar pressure. Half of the pillar cross-section is shown. A comparison of the simulated mechanical behavior is shown in Table 3.3.

The simulation results in Fig. 3.5 illustrate the impact of the high pressure of the overmolding process on the thin film packages. To guide the structural design of the micropackages, failure limits are defined according to the microsystem requirements and the package material properties. The failure limits shown in Fig. 3.5 represent the headroom required for the microsystem operation (max downward cap deflection of 2 µm), and the ultimate stress of the silicon nitride sealing layer (1 GPa), beyond which the material is expected to fracture. Furthermore, introducing a supporting pillar of 20 µm diameter at the package center significantly reduces the deformation under high pressure while maintaining a similar stress level in the cap. The discrepancy between the analytical model and the FEM simulations is mainly attributed to the different 3D geometry and edge conditions. For the analytical model perfectly fixed (or clamped) edges were used, whereas for the FEM the 3D edge geometry shown in Fig. 3.3 was used. Moreover, only the FEM results include the effect of the composite cap structure, the orthotropic behavior of PAA and the nonlinear behavior of the Al layer.

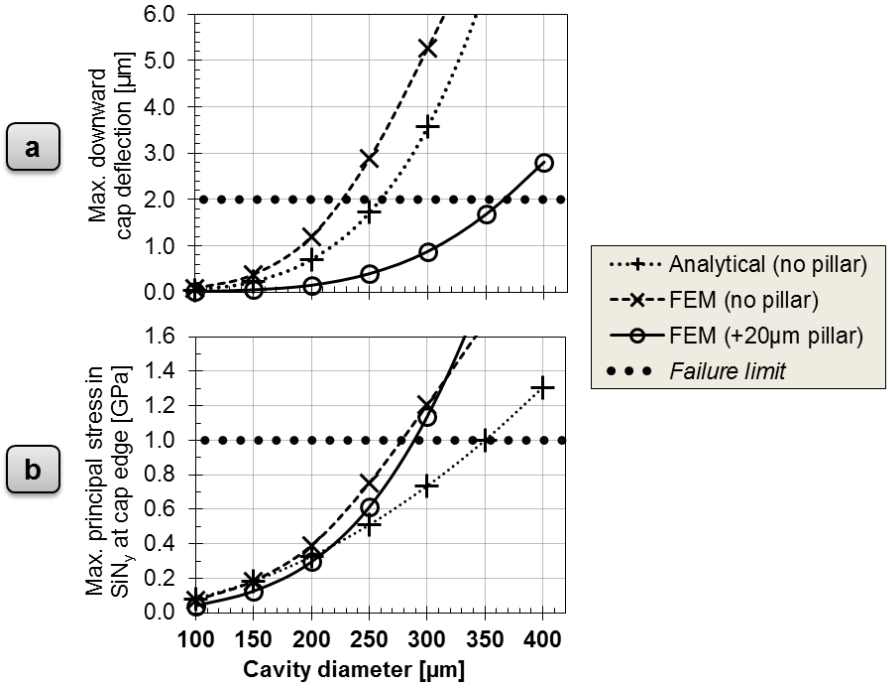


Fig. 3.5 Simulated response of circular thin film packages of 8.3 µm cap thickness and varying diameter subjected to a differential pressure of 30 bar: (a) central cap deflection; and (b) maximum edge stress. The results are obtained using the analytical formulas in Table 3.1 together with the material properties in Table 3.2 and the FEM shown in Fig. 3.3.

3.3.2 Residual stresses and temperature variations

Different mechanisms give rise to residual stresses in thin films, although they are mainly attributed to post-deposition rearrangement of the atoms or molecules of the film. Extra stresses are also induced as a result of the mismatch in the thermal expansion coefficients of different films in contact. Moreover, the presence of a ductile material (Al) in the structure can result in an evolution (or memory) effect due to the irreversible plastic deformation of this ductile material when stressed beyond its yield stress limit (0.12 GPa).

To demonstrate the impact of residual and thermally-induced stresses on PAA-based micropackages, Fig. 3.6 shows finite element simulation results for the cap center deflection of a circular package under 1 bar differential pressure during 20 successive cycles of temperature variation between -55 °C and +125 °C. The simulated package consists of a 6 µm-thick cap (2 µm

Al/PAA + 4 µm SiN_z) of 250 µm diameter, 5 µm cavity height, 60° edge inclination angle and no supporting pillar. The results are shown for the two different situations for the residual stresses in the cap at the beginning of the first temperature cycle at room temperature: **(a)** no residual stresses in any of the cap layers; and **(b)** tensile stress of 50 MPa in the Al and nanoporous alumina (PAA) layers, and compressive stress of 100 MPa in the silicon nitride (SiN_z) sealing layer.

The results in Fig. 3.6 show the simulated impact of both residual stresses and ambient temperature on the package deformation. In the case of no initial stresses in the cap layer (Fig. 3.6(a)), the result is a downward cap deflection under the external pressure as illustrated in (Fig. 3.6(c)). The downward deflection of the cap increases even more at lower temperatures due to the thermal expansion mismatch between the cap layers and the underlying Si substrate. When lowering the temperature, the cap tends to shrink more that the substrate and therefore its volume is reduced causing a downward deflection. The repeated temperature cycling between -55 °C and +125 °C further causes an evolution or drift in the cap deflection. This is attributed to the memory effect caused by the plastic deformation of the Al portion of the cap when its stress reaches the yield limit (0.12 GPa). Finally, the change of the cap deformation (at a given temperature) seems to stabilize after a number of temperature cycles as the Al structure tends to deform in a way that prevents it from reaching the yield limit again (given that the loading is similar in all cycles).

In the case of an initial or residual stress in the cap (Fig. 3.6(b)), the simulation results show a different behavior compared to the previous case. The initial value as well as the evolution of the cap deflection is more inclined towards the positive (or upward) direction (resulting in a dome-shaped cap as shown in Fig. 3.6(d)). Despite applying 1 bar of pressure on the top side of cap, the initial deformation at room temperature is close to zero. This is mainly attributed to the relatively large compressive stress in the sealing layer (100 MPa) which counteracts the tension caused by the external pressure as illustrated in Fig. 3.6(d). This value of the residual stress for SiN_z can actually be obtained using a typical PECVD fabrication process (Martyniuk *et al.*, 2004). Moreover, the typical tensile residual stress (50 MPa) in the Al and PAA layers causes a bending effect at the cap edge (see Fig. 3.6(d)) which promotes the upward deformation of the cap. Furthermore, the deflection dependence on the ambient temperature is driven by the thermal expansion mismatch between the cap and the substrate. In this case, increasing the temperature causes more expansion in the cap, and hence more upward deflection. As in

the previous case, plastic deformation in the Al layer results in an evolution in the cap shape with the repeated temperature cycles. Again this evolution tends to stabilize due to the deformation of Al to a "lower energy" shape where it barely reaches its yield limit with the progression of the loading cycles.

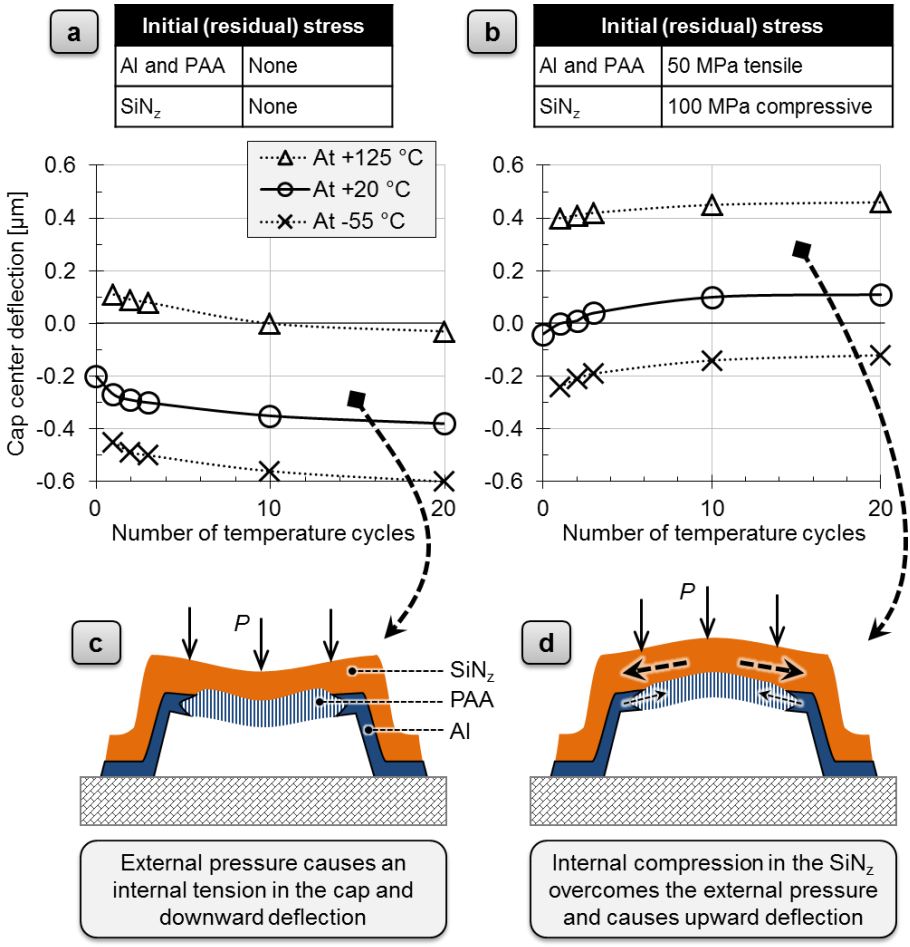


Fig. 3.6 (a,b) FEM simulation results of the cap center deflection (with two different initial conditions for the residual stresses) for a circular micropackage of 250 µm cavity diameter and 6 µm cap thickness under 1 bar hydrostatic pressure during 20 temperature cycles (-55 °C to +125 °C); (c,d) Schematic illustrations of the downward (negative) cap deflection due to the external pressure load and the upward (positive) deflection due to internal stresses in the cap.

It is worth mentioning that the increased distance between the cap and the substrate (as in Fig. 3.6(d)) is a desired outcome since it reduces any capacitive coupling between the cap and the underlying RF circuit. Moreover, the dome-shaped cap enhances the cap rigidity against external hydrostatic loads. However, in order to avoid mechanical instability (buckling) of the structure, the overall compressive stress in the cap layers should remain below a critical value (σ_{cr}). The lower limit for this critical stress can be estimated for the case of a circular plate with perfectly clamped edges using the formula (Shames and Dym, 1995):

$$\sigma_{cr} = \frac{14.65\, E\, t^2}{12\, d^2\, (1-\nu^2)} \tag{3.7}$$

Where E is the equivalent Young's modulus of the plate, t is the plate thickness, d is the plate diameter and ν is Poisson's ratio. Equation (3.7) yields a critical compressive stress value close to 390 MPa for a circular cap of 6 µm thickness (2 µm PAA + 4 µm SiN_z) and 250 µm diameter. Therefore, the introduction of a compressive stress that is lower than this value into the sealing layer is not expected to cause buckling of the cap structure.

3.4 Tested performance under hydrostatic loads

3.4.1 Hydrostatic stress test

In order to evaluate the ability of the thin film packages to withstand the high pressure levels employed in an epoxy overmolding process, a hydrostatic stress test is applied to selected samples of *Configuration II-B* with a cap thickness of 8.3 µm and cavity diameters in the range of 200 to 400 µm (as in Fig. 2.16 and Fig. 2.20). In this test, the thin film packages are optically inspected before and after immersion in deionized water at a pressure of 30 bar and subsequently at a pressure of 90 bar for a short duration (less than 10 minutes in each case). An example of the obtained results is shown in Fig. 3.7. By inspecting six specific micropackages using a microscope before starting the test, three sealed (intact) packages are found in addition to two packages with intentional vent holes (not sealed during the fabrication process) and one package with an unintentionally damaged cap as shown in Fig. 3.7(a).

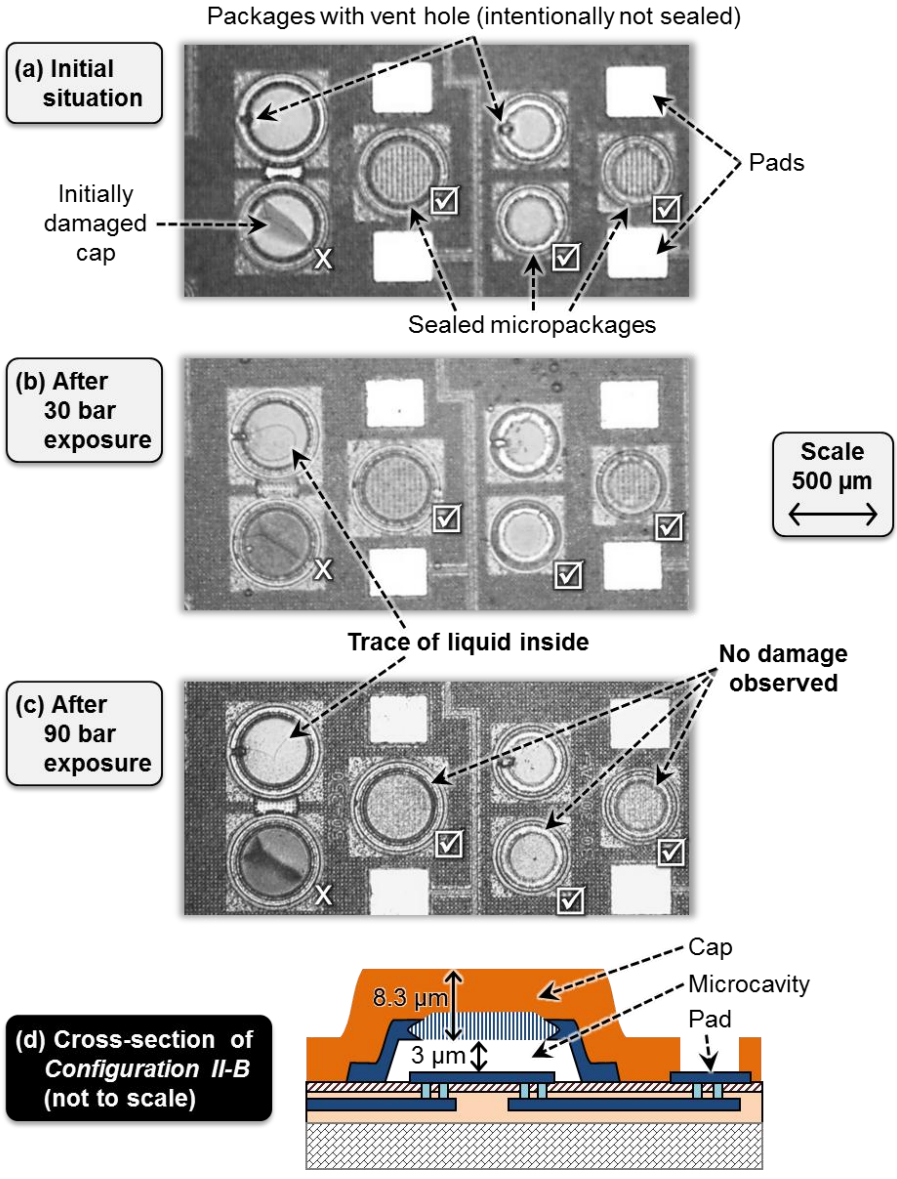


Fig. 3.7 (a-c) Top-view micrographs of a set of six circular thin film packages at the different stages of a hydrostatic stress test in deionized water; and (d) a cross-sectional-schematic showing the structure of the micropackages used in this test (*Configuration II-B* as in Fig. 2.16 and Fig. 2.20).

After exposing all the micropackages to a hydrostatic pressure of 30 bar in deionized water, the samples are dried and inspected again. It is observed that the three sealed packages remain intact after the hydrostatic stress test but a trace of a fluid (water) can be seen inside one of the unsealed packages as shown in Fig. 3.7(b). The same packages are then exposed to a second stress test under 90 bar in deionized water. Again after drying the sample and inspecting it, no physical damage can be seen in the sealed packages while a trace of water remains in one of the unsealed packages (see Fig. 3.7(c)). Despite being physically intact after the hydrostatic stress test, the micropackages are expected to undergo a significant vertical displacement under such large loads (according to the models described earlier). This indicates a rather high flexibility of the thin caps in accommodating such large deformations (note that the maximum allowed downward deformation of the caps in this case is approximately 3 μm which is the cavity height).

3.4.2 Package encapsulation using epoxy overmolding

In a different experiment to validate the compatibility of the micropackages with epoxy overmolding, two samples of an approximate size of 20×200 mm^2 are diced out of 200 mm wafers with a large number of micropackages of *Configuration II-B* (as in Fig. 2.16 and Fig. 2.20). These samples are then subjected to an epoxy overmolding process at two different transfer pressures of 30 and 90 bar. The overmolding process is performed at a maximum temperature of 175 °C in a manual transfer molding machine. This test was provided as a research service by Fico-BESI (part of BE Semiconductor Industries N.V.) in The Netherlands, in the frame of MEMSPACK project (www.memspack.eu). A commercial black epoxy compound featuring a relatively low thermal expansion coefficient (< 50 ppm/K) is chosen for this test in order to reduce the thermomechanical mismatch with the Si substrate. The final compound thickness on top of the thin film packages is in the range of 50 to 200 μm.

After the overmolding process, the samples are subjected to a standard inspection test for electronic packages based on scanning acoustic microscopy (SAM). Neither large introduced defects nor additional air voids are detected in the SAM images at the interface between the epoxy compound and the encapsulated samples. However, the low resolution of SAM and its sensitivity to the presence of voids (the microcavities) make it less efficient to detect small defects in the thin film packages. Therefore, the samples were later manually cleaved and thoroughly inspected by high-magnification scanning electron microscopy (SEM), yielding the results shown in Fig. 3.8 and Fig. 3.9.

In both cases, no substantial physical damage is observed in the thin film packages (confirming the observations from the SAM inspection and the hydrostatic stress test results shown in Fig. 3.7).

The package anchor, the thin cap, and the 220 µm-wide cavity shown in Fig. 3.8 appear to be perfectly intact after the epoxy overmolding process at 30 bar. In this case, the cavity height after the overmolding process is measured at 3 µm which is the same expected height before this process. This means that the micropackage experienced almost no deformation under the high pressure and temperature of the overmolding process. Although simulations predict a downward deflection of 1 µm at the cap center under 30 bar pressure at room temperature, the fact that the overmolding process is performed at a high temperature (175 °C) results in a compensating upward deflection due to the mismatch in thermal expansion of the cap compared to the substrate (see Fig. 3.6). Other effects which are not determined here include the residual stress in the cap layers. As mentioned earlier, a compressive stress in the cap layers can further reduce the downward deflection during the overmolding process

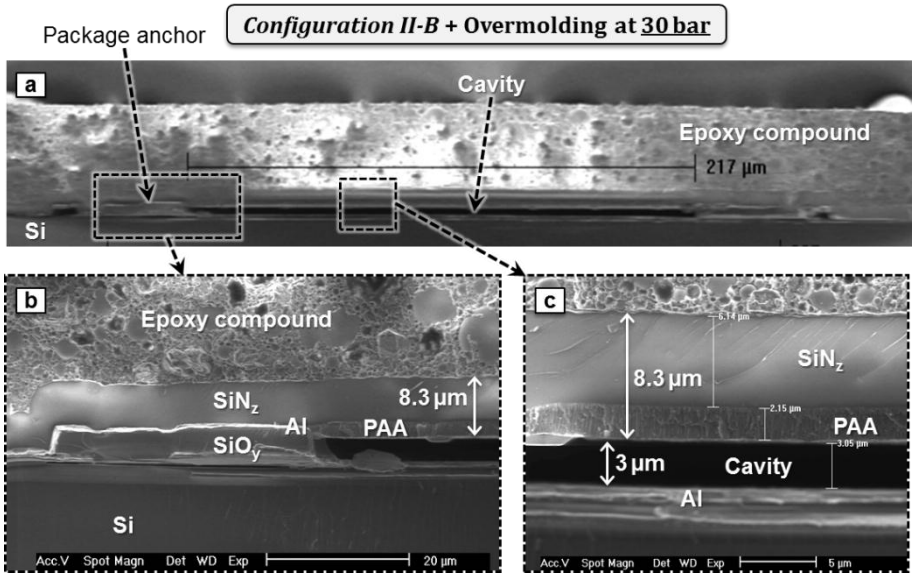


Fig. 3.8 Cross-sectional SEM views of a circular thin film package of ~220 µm cavity diameter after epoxy overmolding at 30 bar: (a) Full view of the thin film package encapsulated in the epoxy compound; (b) Close-up view of the package anchor; (c) Close-up view near the center of the package showing the normal height and integrity of the microcavity.

In another sample, a thin film package featuring a 240 µm-wide cavity appears to be collapsed after the epoxy overmolding process at 90 bar as shown in Fig. 3.9. This collapse of the thin film package is proven by the residues of the cap material (PAA) observed on top of the packaged metal (Al) interconnects, as shown in Fig. 3.9(c). Furthermore, a vertical deflection of approximately 3.5 µm is expected at the cap center from simulations of the overmolding process (assuming no residual stress in the cap at room temperature). This deflection is larger than the typical cavity height (3 µm) and therefore explains the apparent contact between the cap and the underlying Al layer on the substrate. As previously mentioned, this cap deformation during the epoxy overmolding process can be limited by reducing the cavity diameter or by introducing one or more supporting pillars to the package structure.

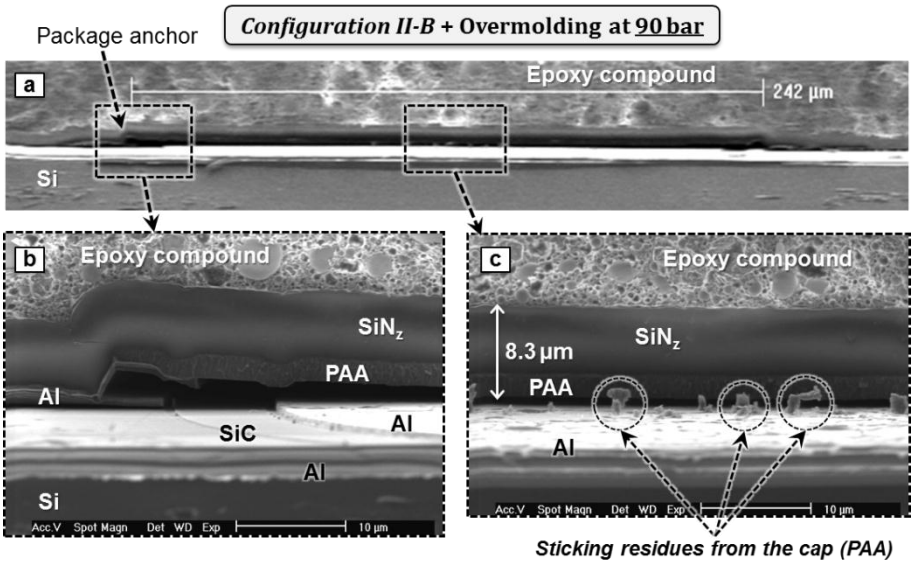


Fig. 3.9 Cross-sectional SEM views of a circular thin film package of ~240 µm cavity diameter after epoxy overmolding at 90 bar: (a) Full view of the thin film package encapsulated in the epoxy compound; (b) Close-up view near the package anchor showing the significant downward cap deformation; (c) Close-up view near the package center showing the thin cap collapse, and small residues of the PAA membrane adhering to bottom-side of the cavity.

3.5 Conclusions

The thermomechanical behavior of thin film packages realized using nanoporous alumina membranes is associated with complex phenomena like the anisotropic behavior of nanoporous alumina and the ductile (non-linear) behavior of Al thin films. These and other details are incorporated in analytical and finite element models which are used to understand the thermomechanical behavior of the thin film packages. This understanding is essential to achieve the goal of constructing strong and reliable on-wafer micropackages. It has been shown from basic analytical models that circular packages experience less deformation and less stress concentration compared to traditional square or rectangular packages of similar dimensions under the same loading conditions.

More complex models show the significant impact of the structural design of a micropackage (its dimensions, the presence of a supporting pillar and the inclination angle of the edges) on its response to a hydrostatic load. Simulation results further show that the micropackages can withstand extreme temperature variations (*e.g.*, between –55 °C and +125 °C) under atmospheric pressure. Moreover, the initial (or residual) stresses in the thin films of the cap can have a considerable impact on the shape, strength and durability of the micropackages. For example, an upward cap deformation (against the applied external pressure) can be achieved by introducing a compressive residual stress of 100 MPa in the nitride sealing layer and a tensile residual stress of 50 MPa in the Al and PAA layers.

Finally, both simulations and experimental evidence show that carefully designed micropackages can withstand the rather harsh process of epoxy overmolding performed at a temperature of 175 °C and hydrostatic pressures of 30 bar. The micropackages can even withstand a similar overmolding process at a higher pressure (90 bar), although significant cap deformation takes place for micropackages of typical diameters (>0.2 mm). By adjusting the cap dimensions or the use of one or more supporting pillars, such large deformations can be reduced.

"Gold there is, and rubies in abundance, but lips that speak knowledge are a rare jewel."

Proverbs of Solomon 20:15

Chapter 4 Hermeticity and reliability

This chapter starts with an outline of the main sources of environmental changes in small cavities. Next, the different existing methods to evaluate the hermeticity of micropackages are briefly compared to identify the most suitable techniques for thin film packages. This is followed by a detailed hermeticity investigation of the micropackages using an optical detection method of the cap deformation. The feasibility of using miniature pressure sensors that can be embedded inside the micropackages is then discussed. Finally, the results of four different reliability tests applied to the PAA-based thin film packages are presented, providing more insight into the robustness of these microstructures.

4.1 Introduction

4.1.1 Sources of environmental changes in small cavities

As previously discussed in Chapter 1, a majority of modern microsystems require a relatively low pressure to properly function (see Table 1.1). It has further been shown in Chapter 2 that such low pressures can be established in a thin film package by means of a deposition process of a sealing layer under low pressure. However, establishing the low pressure during the sealing process is not a guarantee that the internal package environment will not change afterwards. The evolution of the internal environment of a thin film package can be caused by different transfer mechanisms of mobile molecules (gases or vapors) as illustrated in Fig. 4.1.

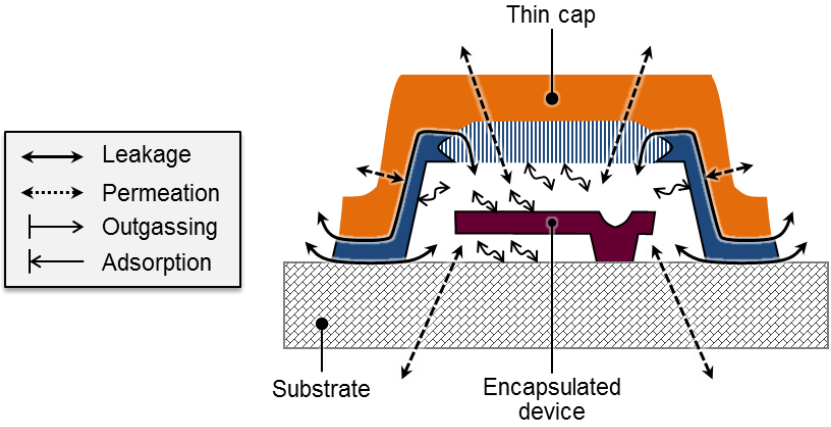


Fig. 4.1 A schematic illustration of the main transfer mechanisms of mobile molecules (like gases or vapors) into and out of the microcavity of a thin film package based on nanoporous alumina.

A common mechanism of gas or vapor transfer into a cavity is leakage through small channels that are typically formed at the interfaces between different materials due to imperfect adhesion or mismatch in surface roughness. Theoretical models have already been developed to explain the relationship between the leak rate of a certain gas and the geometry of the leakage path (Davy, 1975). Another common mechanism of molecules transfer is permeation through the encapsulation materials or the underlying substrate. It is known that certain materials, including metals and ceramics, are more resistant to permeation compared to other materials like plastics and epoxies (Traeger, 1977).

Leakage and permeation influence the internal environment of a package through an exchange of molecules with the outside environment, whereas other mechanisms can influence the internal environment regardless of the external conditions. Such mechanisms include the outgassing of different mobile molecules from the internal surfaces of the microcavity. The opposite mechanism is also valid where mobile molecules are adsorbed back into the internal surfaces of the microcavity. Outgassing is a rather complex phenomenon that is related to the detailed composition of the materials present inside the cavity, their method of construction, and their history of exposure to certain fluids and/or high temperatures (Moraja, 2011).

Several techniques can be used to quantify the influence of the above mentioned gas or vapor transfer mechanisms on the internal environment (or

pressure) of the thin film packages as discussed hereafter. Moreover, by understanding the cause of an undesired change to the internal cavity environment, one can devise methods to eliminate or mitigate this undesired change. For example, leakages can be limited by reducing the number of exposed interfaces at the package edge and or increasing the length of the sealing ring (as discussed later in this chapter). Permeation can be reduced by using a denser or thicker sealing layer (Traeger, 1977). Outgassing can be overcome by carefully choosing the deposition processes of the internal package materials and/or by using a high temperature anneal (bake out) of the packages directly before the sealing process (Wang *et al*., 2011). Finally, the use of a getter material inside the microcavity is another interesting method to achieve a stable and very low pressure (Boffito et al., 1981). This last method is however more challenging in terms of integration with thin film packages due to the need for a special metal alloy (*e.g.*, Zr-Ni, Zr-Al or Zr-V-Fe) which requires a dedicated space inside the microcavity and imposes a number of constraints on the encapsulation process flow.

4.1.2 Methods of hermeticity evaluation

As illustrated in Table 4.1, a variety of methods have already been reported for the purpose of hermeticity evaluation for small (electronic) packages. These include methods based on the physical observation of flowing gas bubbles or molecules (methods (1) to (5) in Table 4.1), optical detection of certain gas traces (methods (6) and (7)), optical or electrical detection of the cap deformation (methods (8) and (9)), as well as electrical methods which make use of a special microsensor embedded inside the package (methods (10) and (11)). Table 4.1 further provides an estimate of the range of leak rates that can be measured by each method and its main requirements or limitations according to existing literature. Examples of literature references discussing each hermeticity evaluation method are also mentioned in Table 4.1, where more details and specific applications can be found.

Table 4.1 An overview of the commonly used methods to test the hermeticity of vacuum micropackages (partially adapted from Costello *et al*., 2012).

Testing method	Literature reference(s)	Measurable leak rate [mbar.l/s]	Test requirements and conditions
(1) Perfluorocarbon gross leak test	MIL-STD-883H (Method 1014.13, Condition C)	$>10^{-4}$	Large cavity volume
(2) Tracer gas He fine leak test	MIL-STD-883H (Method 1014.13, Cond. A_1 and A_2)	$10^{-10} – 10^{-6}$	Large cavity volume
(3) Through-hole He leak test	Jourdain *et al*., 2005	$10^{-12} – 10^{-3}$	Hole drilling through the substrate (destructive)
(4) Radioisotope gross/fine leak test	MIL-STD-883H (Method 1014.13, Cond. B_1 and B_2)	$>10^{-12}$	Large cavity volume
(5) Residual gas analysis	Moraja, 2011	$>10^{-12}$	Large cavity; complex analysis; cap detachment (destructive)
(6) Fourier-transform IR spectroscopy	Nese *et al*., 1996	$10^{-12} – 10^{-8}$	Specific gas (*e.g.*, N_2O); IR transparency
(7) Optical transmission of oxidized metal	Gueissaz, 2005	$>10^{-16}$	Embedded thin Cu; oxidizing environment; IR transparency
(8) Optical gross/fine leak test based on cap deformation	MIL-STD-883H (Method 1014.13, Cond. C_4 and C_5); Elger *et al*., 2004; this thesis	$>10^{-16}$	Low cap stiffness; reflective cap surface
(9) Capacitive cap deformation test	Wang *et al*., 2012	$>10^{-18}$	Small cavity height; conductive cap; embedded electrode
(10) Micro-Pirani gauge	Stark *et al*., 2005; Topalli *et al*., 2009	$10^{-16} – 10^{-8}$	Embedded sensor (design depends on the cavity pressure)
(11) Microresonator Q-factor	Gui *et al*., 1995; Li *et al*., 2009	$10^{-18} – 10^{-10}$	Embedded sensor (design depends on the cavity pressure)

Each of the methods mentioned in Table 4.1 has its own advantages and disadvantages. Generally speaking, the methods based on quantifying the amount of gas leaking out of or into a micropackage (methods (1) to (6)) have a relatively limited precision. In other words, these methods cannot detect the ultra-small amount of leakage expected in a thin film package with a cavity volume less than 10^{-12} m^3 (or 1 nl). Other methods which can detect smaller leakages have their own limitations as indicated in Table 4.1. For example, method (7) is based on detecting the thickness of a copper oxide layer as an indication of the amount of oxidizing molecules present in the cavity. This method is therefore rather indirect and is influenced by the specific properties of the leaking gas and the contents of the cavity. Furthermore, other testing methods based on an embedded microstructure or pressure sensor (methods (9) to (11)) can provide precise leak rate measurements. However, these methods are inherently complex due to the need for a special embedded microstructure. On the other hand, method (8) which is based on an external optical detection of the deformation of a thin cap seems to provide the best compromise between precision and simplicity (Elger *et al*., 2004). This will be the main method used for the hermeticity assessment of the new micropackages based on nanoporous alumina as discussed in the next section. Moreover, the feasibility of using embedded sensors (like a microresonator or Pirani gauge) is also discussed later in this chapter.

4.2 Hermeticity testing based on cap deformation

A simple and effective method for hermeticity testing of thin film packages makes use of the cap deformation to detect changes in the internal package pressure (Elger *et al*., 2004; Wang *et al*., 2012). This method is also incorporated in the optical gross/fine leak test conditions of the US military standard on microcircuits testing (MIL-STD-883H, method no. 1014.13). The cap deformations can be detected optically using an interferometer (Elger *et al*., 2004; Hariharan, 2006) or electrically through changes in the capacitance between the thin cap and an underlying electrode—provided the cap is partially made of a conductive material—(Wang *et al*., 2012). Given that most micropackages discussed in this thesis are constructed using dielectric materials (nanoporous alumina and silicon nitride), the optical detection technique is preferred. However, a requirement of the optical detection technique is to have an optically reflective surface of the caps to facilitate the interferometry measurements. Hence, all micropackages tested using this method are first covered with a very thin sputter-deposited Ti layer (30 nm). The thickness of this Ti layer is chosen to be as small as possible to provide a

minimal amount of optical reflection without having a significant impact on the hermeticity of the micropackages. Although the absolute impact of this thin Ti layer on the hermeticity of the packages is not known, the relative performance of different package designs and configurations tested in the same way is considered to be accurate. In order to find out the exact impact of such thin Ti layer on hermeticity, another testing method can be used as reference (for example, using an embedded pressure sensor as discussed later in this chapter).

The amount of gas leakage (or leak rate) in a small package can vary in a wide range depending on the effectiveness of its sealing. A distinction can be made between large (or gross) leaks in a package that is improperly sealed (or damaged) and small (or fine) leaks in other cases where a package is properly—but not perfectly—sealed (see Fig. 4.1). In this context, one may define a gross leak as what causes a micropackage to immediately follow variations in external pressure (in less than one minute), while a fine leak is what causes a gradual change in the internal environment of the package within a relatively long period (more than a day). Considering the small cavity volume of a thin film package (*e.g.*, 1 nl) and a typical differential pressure close to 1 bar, the above definition would correspond to leak rates above 10^{-8} mbar.l/s being gross leaks and leak rates below 10^{-11} mbar.l/s to be considered as fine leaks. In the following subsections, the methods and results of two different tests for gross leak and fine leak evaluation based on optical detection of the deformation of thin caps are discussed in more details.

4.2.1 Gross leak test in air

To evaluate the proper sealing (or gross-leak tightness) of micropackages created using nanoporous alumina membranes and silicon nitride sealing, chips of approximately 2×2 cm^2 area with a large number of thin film packages are placed in a sealed chamber which is optionally connected to a vacuum pump as shown in Fig. 4.2. In this experiment, the profile (or top surface height) of a number of the thin film packages is measured using an optical interferometer before and after the chamber pressure is changed from atmospheric pressure (1 bar) to a lower pressure (approximately 0.2 bar). As mentioned earlier, a 30 nm-thick Ti layer is sputter-deposited on top of the thin film packages before starting this hermeticity test to provide sufficient optical reflection for the white light interferometry measurements.

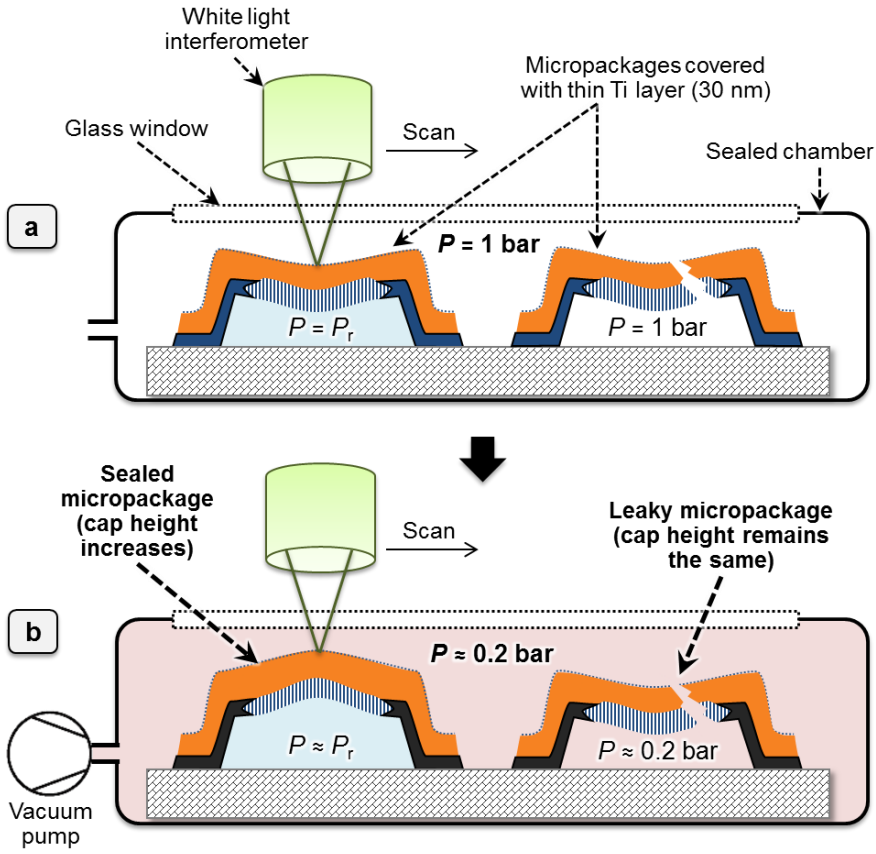


Fig. 4.2 Cross-sectional schematics illustrating the method used for gross leak testing by optical detection of the cap deformation of thin film packages: (a) the height profile of the packages is measured under atmospheric pressure (1 bar); and then (b) the same measurement is repeated under lower pressure (around 0.2 bar).

Gross-leak tightness, as defined above, is observed when the thin caps deflect instantaneously upwards in response to the external chamber pressure reduction (see the package on the left side in Fig. 4.2). The amount of cap deflection expected in this test can be estimated using either the analytical or finite element models discussed in Chapter 3. The cap deflection is a result of a change in the differential pressure on the cap, implying that the internal package pressure does not undergo a significant change during the test (*i.e.*, no large or gross leakage takes place). A comparison between the measured and simulated cap profiles for a properly sealed circular thin film package

under atmospheric and low pressure is shown in Fig. 4.3. The package has a cavity diameter of 400 µm and a cap thickness of 6 µm (according to *Configuration I-B* as in Fig. 2.14(b)). For the finite element simulations, it is assumed that the sealing layer has a residual compressive stress of 100 MPa and the PAA and Al layers have a tensile residual stress of 50 MPa. It is further assumed that the cavity pressure is always much lower than the test chamber pressure. Moreover, it is possible to determine the effective Young's modulus of sealed micropackages from this experiment. This can be done using the analytical formulas in Table 3.1 and by knowing the cap dimensions, the change in the applied external pressure and the corresponding measured cap deflection.

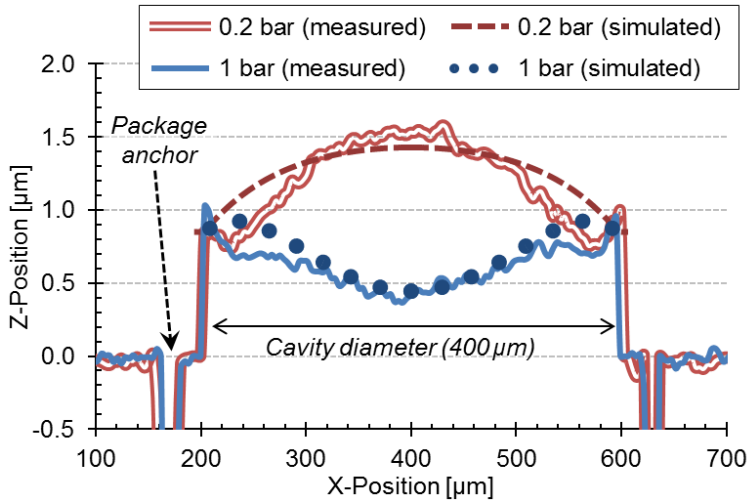


Fig. 4.3 An example of the measured and simulated height profile for a circular micropackage under an external pressure of 0.2 and 1 bar (as used in the gross-leak test in Fig. 4.2). In this case the cap deforms in response to the change in external pressure which indicates the package is sealed (gross-leak tight). Simulations are performed using the FEM in Fig. 3.3.

On the other hand, a micropackage that is damaged or improperly sealed (with a leak rate above 10^{-8} mbar.l/s) undergoes no substantial deformation during the gross leak test as shown for the package on the right side in Fig. 4.2. In this case a large leakage path exists between the inside of the package and its surroundings, leading to a small or no differential pressure across the cap (irrespective of the change in the surrounding pressure).

The gross leak test described above is only intended for a qualitative assessment of the hermeticity (or proper sealing) of the micropackages. Thin film packages that pass this test with a positive result (as in Fig. 4.3) can then be submitted to a more extensive hermeticity assessment using the fine leak test described below.

4.2.2 Fine leak test in helium and air

The method developed here for fine leak testing makes use of the same principle of optical detection of the thin cap deformation as explained earlier for the gross leak test. Furthermore, two different variants of the fine leak test have been applied to a number of micropackages. The first variant of the fine leak test is based on an accelerated exposure to helium (under a high pressure of 3 bar) followed by monitoring of the outward leakage of He from the micropackages as shown in Fig. 4.4.

The helium leak test begins with measuring the initial (reference) cap height of certain packages in air (Fig. 4.4(a)). Next, the samples are stored for 2 to 3 days in a sealed chamber filled with He under 3 bar pressure to allow a relatively large amount of He to leak (or permeate) into the packages (Fig. 4.4(b)). The chips are then removed from the pressurized He chamber and the cap height of the same packages is immediately measured in air (Fig. 4.4(c)). The internal helium partial pressure of the packages is then obtained by comparing the latter measurement to the initial cap profile before storage in He. Next, similar measurements of the cap profile are taken within a period of few hours up to several days to monitor the outward leakage (or permeation) of He from the packages which are stored in air after their exposure to the high He pressure (Fig. 4.4(d)).

An example of the evolution of the measured cap center height (y_c) for a circular thin film package of 350 µm cavity diameter and 30 µm sealing ring width (of *Configuration II-A* as in Fig. 2.16 and Fig. 2.19) during the different phases of the He leak test is shown in Fig. 4.4(e). Given that the stiffness of the cap is known, this cap height evolution can be translated into pressure changes in the microcavity using an analytical model as described hereafter. This results in a calculated evolution of the cavity pressure (relative to the reference pressure P_r) as shown in Fig. 4.4(f). The obtained changes in the cavity pressure illustrate the inward He leakage (pressure increase) during the package storage under 3 bar of helium pressure (the cavity pressure increases by 2.4 bar after the He "filling" phase). This is followed by a fast (exponential) decrease in the cavity pressure as the He leaks out of the cavity.

The fact that the partial pressure of He in air is very low (less than 1 Pa, or 0.01 mbar) results in an almost complete outward leakage of the He that was introduced in the cavity during this test. This can be illustrated by the low cavity pressure which almost returns to the reference pressure at day 13 as shown in Fig. 4.4(f). Therefore, the packages submitted to the He leak test can be further tested using the (long-term) air leak test as discussed below.

In the other variant of the fine leak test, the cap heights of the micropackages are regularly monitored while the samples are stored for a long period (up to 14 months) under 1 bar of air pressure (at 40% to 60% relative humidity) as shown in Fig. 4.5(a,b). As discussed previously for the He fine leak test, a reference measurement of the cap height is initially performed to be able to calculate the subsequent changes in the cavity pressure during storage in air. An example of the cap height evolution and the corresponding changes in the cavity pressure during this air leak test are shown in Fig. 4.5(c,d) for the same circular package used to obtain the results in Fig. 4.4(e,f) (*Configuration II-A* with 350 µm cavity diameter and 30 µm sealing ring width).

The results in Fig. 4.4(e,f) and Fig. 4.5(c,d) further show the expected error range of the measured cap deflection (±50 nm) and the corresponding pressure change. This error range includes the measurement uncertainties related to the cap surface roughness (see the measured cap profile in Fig. 4.3) as well as the finite precision of the optical interferometry measurement.

For the helium- and air-based fine leak tests described above, changes in the internal pressure of the packages and the corresponding leak rates can be calculated based on the measured deformation of the thin caps. Assuming a perfectly clamped cap membrane and small deflections, the change in the differential pressure (ΔP) across the cap—which is the same as the change in the cavity pressure, given the external pressure is fixed at 1 bar—can be estimated by rewriting the analytical formula for cap deflection of a circular package (see Table 3.1) as follows:

$$\Delta P = \Delta y_c E t^3 / 0.0107 {d_C}^4 \tag{4.1}$$

where Δy_c is the corresponding vertical deformation measured at the cap center, t is the total cap thickness, d_C is the cavity diameter and E is the equivalent elastic modulus of the cap membrane.

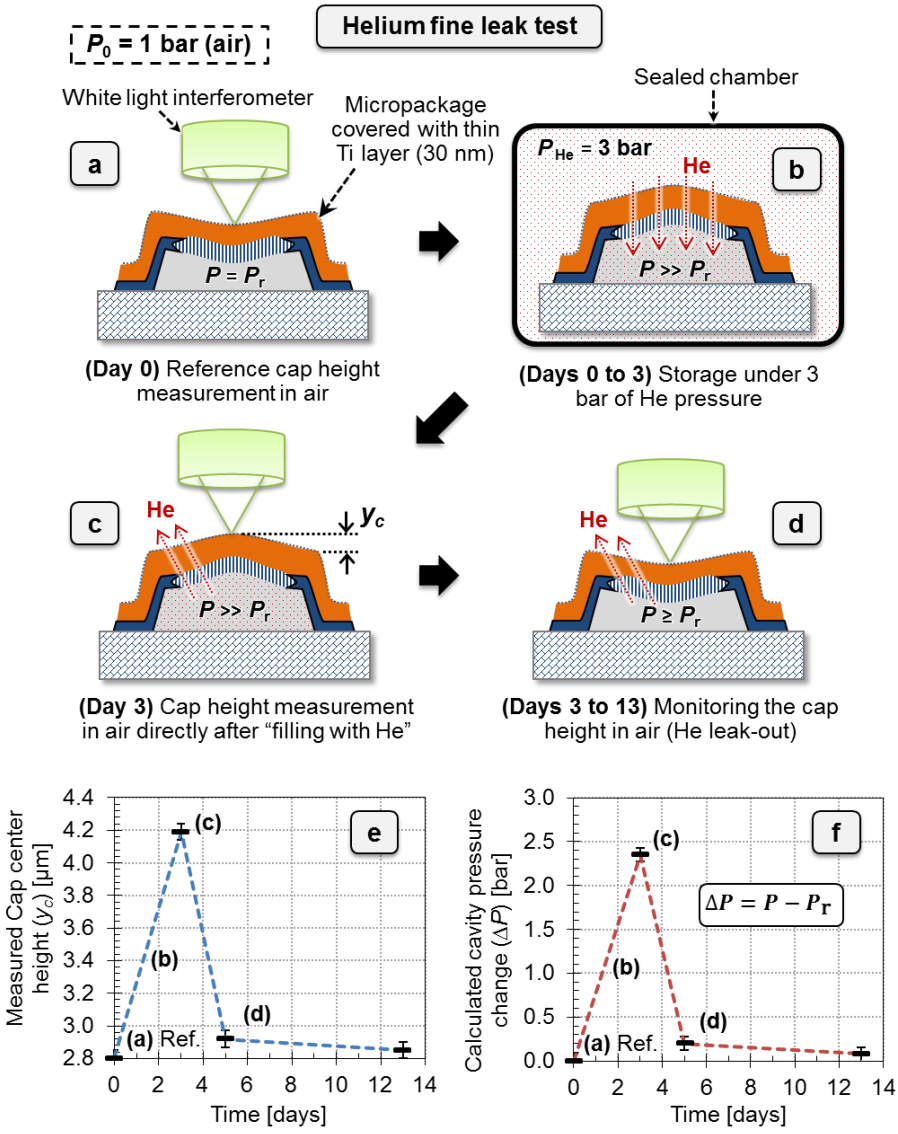


Fig. 4.4 (a-d) Schematics illustrating the main steps of the He fine leak test; (e) the measured cap height evolution during the test; and (f) the corresponding changes in cavity pressure (calculated from equation (4.1)). The results in (e,f) are for a circular thin film package of 350 µm cavity diameter and 30 µm sealing ring width (*Configuration II-A* as in Fig. 2.19).

To incorporate a realistic estimation of the cap stiffness in this hermeticity model, the value of E for each package under test is experimentally

determined from the optical gross leak test described earlier (see Fig. 4.2). In this gross leak test, he cap deflection (Δy_c) is measured against approximately 0.8 bar change in the differential pressure (ΔP), yielding elastic modulus values (E) between 85 and 165 GPa (using equation (4.1)) for packages of different cap thicknesses, diameters and configurations.

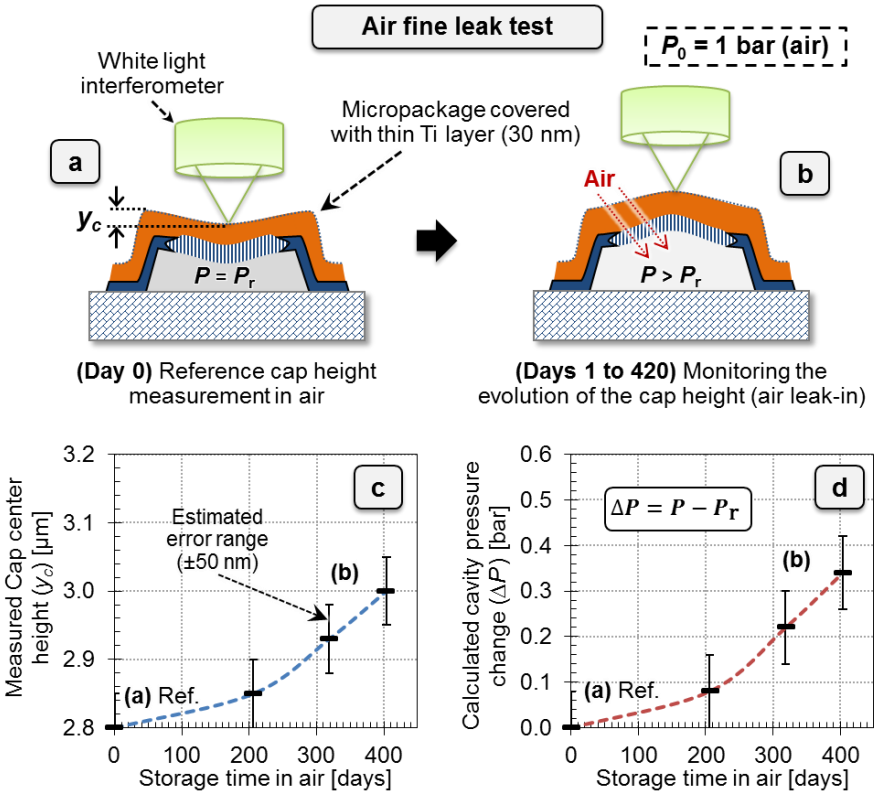


Fig. 4.5 (a,b) Schematics illustrating the main steps of the air fine leak test; (c) the measured cap height evolution during the test; and (d) the corresponding changes in cavity pressure (calculated from equation (4.1)). The results in (c,d) are for a circular thin film package of 350 µm internal diameter and 30 µm sealing ring width (*Configuration II-A* as in Fig. 2.19).

The actual (or measured) leak rate of a certain gas through a certain package is not only dependent on the sealing quality, but also on the differential pressure of the gas, the ambient temperature and the mobility (or size) of the gas molecules (Neyer *et al.*, 2000; Elger *et al.*, 2004). In order to be able to compare the results of different hermeticity tests (where different

gases, pressures or temperatures are involved), an equivalent standard leak rate (L_s) is commonly used (according to MIL-STD-883). This standard leak rate (L_s) is defined as the equivalent of the measured leak rate in a standard environment (dry air at 1 bar and 25 °C). A typical leak rate unit is mbar.l/s which represents an amount of gas at certain temperature (mbar.l) leaking through a package in a unit time (s). It has further been shown that the standard leak rate (L_s) is related to the change in the cavity pressure (ΔP) by the following formula (Elger *et al*., 2004):

$$L_s = \ln\left(\frac{P}{P_1 - \Delta P}\right)\frac{VP_0}{\Delta t}\sqrt{\frac{M_{LG}}{M_A}} \tag{4.2}$$

where P_1 is the partial differential pressure of the leaking gas across the cap at the beginning of the leakage period, V is the internal cavity volume, P_0 is the atmospheric pressure (1 bar), Δt is the time elapsed between the initial and final cap height measurements, M_{LG} is the molar mass of the leaking gas (4 g/mol for He and approximately 28.7 g/mol for air), and M_A is the molar mass of dry air (28.7 g/mol).

For the He leak test, the initial partial differential pressure of He (P_1) can be obtained using equation (4.1) based on the cap profile measurements before and after storage in the pressurized He chamber (*e.g.*, 2.4 bar as in Fig. 4.4(f)). For the air leak test, P_1 is assumed to be equal to 1 bar (*i.e.*, no air exists inside the cavity at the beginning of the test). In equation (4.2), it is assumed that the cavity has a constant volume during the leakage period. Given a small cap deformation, the internal cavity volume (V) is calculated for each package (and for each leak test) by integrating the axisymmetric cap profile ($y(r)$) according to the formula:

$$V = \int_0^{d_C/2} 2\pi r[h_C + y(r)].dr \tag{4.3}$$

where $y(r)$ is approximated as a third order polynomial function, fitted to the average of the initial and final measured cap profiles for the leakage period under study (see Fig. 4.6).

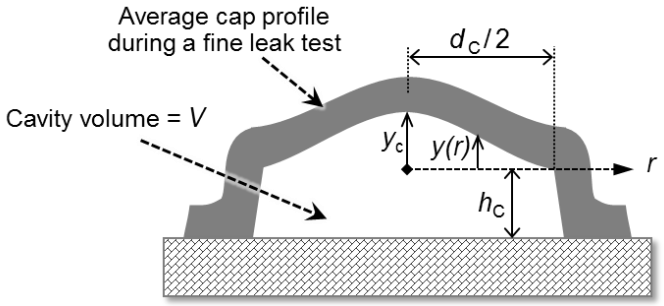


Fig. 4.6 A cross-sectional schematic illustration the geometrical parameters of a thin film package as used in the fine leak model (equation (4.3)).

4.2.3 Hermeticity comparison of different package configurations

By applying the He and air leak testing methods described above (as in Fig. 4.4 and Fig. 4.5) to 5 thin film packages of different configurations, and using equations (4.1 to 4.3), the equivalent standard leak rates in Fig. 4.7 are obtained. All 5 packages are fabricated using nanoporous alumina membranes of 2.0 to 2.3 µm thickness that encapsulate microcavities of approximately 3 µm height (h_C). As shown in Fig. 4.7, three of the micropackages correspond to *Configuration II-A* (as in Fig. 2.16 and Fig. 2.19) with a SiN_z sealing layer of approximately 4 µm thickness, cavity diameter (d_C) of 350 µm and sealing ring widths (w_S) of 10, 20 and 30 µm. Packages of *Configuration II-A* typically feature two levels of Al-based planar interconnects together with tungsten-based vertical plugs. A distinct characteristic of *Configuration II-A* is the aligned edge of both the Al and SiN_z layers forming the package anchor (or sealing ring). Another package reported in Fig. 4.7 corresponds to *Configuration II-B* (as in Fig. 2.16 and Fig. 2.20) with a SiN_z sealing layer of approximately 6 µm thickness, cavity diameter (d) of 400 µm and sealing ring width (w_S) of 20 µm. Similarly, the package of *Configuration II-B* features two levels of Al-based planar interconnects and vertical W plugs. However, the distinctive feature of *Configuration II-B* is the lateral extension of the SiN_z sealing layer beyond the edge of the Al layer at the package anchor. The last package reported in Fig. 4.7 corresponds to *Configuration I-B* (as in Fig. 2.2 and Fig. 2.14(b)) with a SiN_z sealing layer of approximately 4 µm thickness and a cavity diameter (d_C) of 400 µm. *Configuration I-B* features empty micropackages with a sealing ring (Al+SiN_z) that is laterally extending across the whole chip being tested (*i.e.*, in the range of 2 to 10 mm).

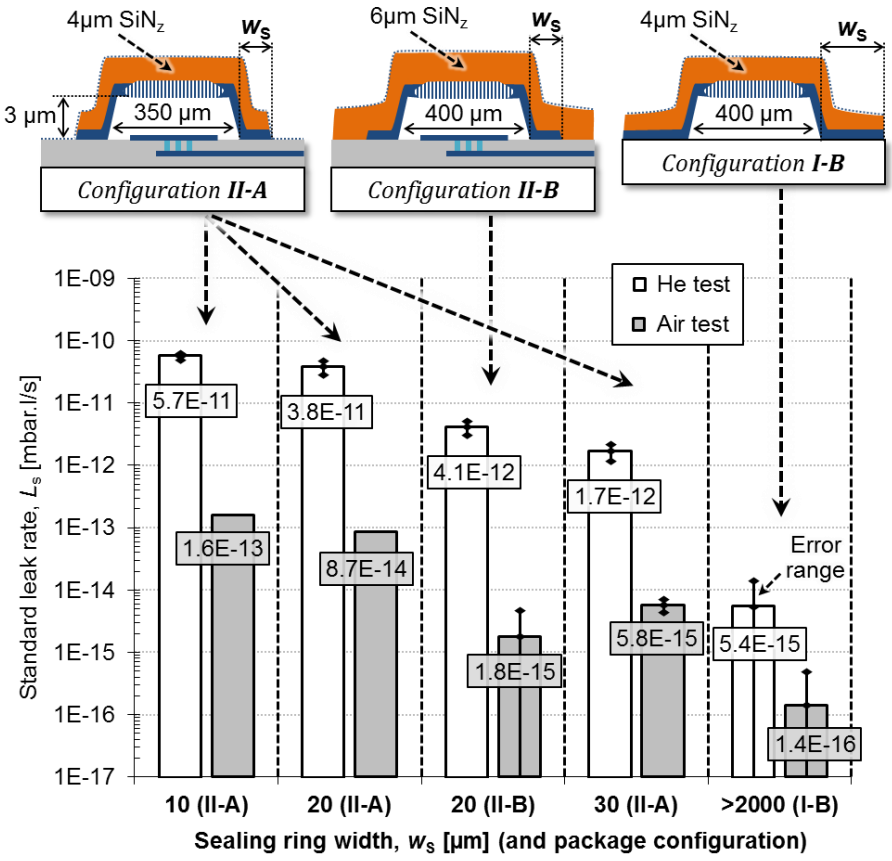


Fig. 4.7 Equivalent standard leak rates extracted from the cap deflection measurements for circular thin film packages of different configurations and sealing ring widths (cavity height is around 3 μm and diameters are between 350 and 400 μm). The detailed construction of these package configurations can be found in Fig. 2.14(b) (*Configuration I-B*), Fig. 2.19 (*Configuration II-A*) and Fig. 2.20 (*Configuration II-B*).

The results in Fig. 4.7 demonstrate the significant impact of changes in the sealing ring width or the package configuration (structure) on hermeticity. The global trend observed in Fig. 4.7 is an almost steady reduction of the observed helium and air leak rates with the increasing sealing ring width (w_S) as in the case of the 3 micropackages of *Configuration II-A*. The He and air leak rates decreased from 5.7×10^{-11} and 1.6×10^{-13} mbar.l/s to 1.7×10^{-12} and 5.8×10^{-15} mbar.l/s, respectively, by increasing the sealing ring width (w_S) from 10 to 30 μm (for the same package diameter, height and structure). This

is attributed to the longer leakage path of gas molecules through the thin film interfaces at the cavity edges for packages with a wider sealing ring.

Moreover, increasing the (silicon nitride) sealing layer thickness and laterally extending it beyond the edge of the Al layer improves the hermeticity of the micropackages. This is proven by the lower He and air leak rates (4.1×10^{-12} and 1.8×10^{-15} mbar.l/s) observed for the package of *Configuration II-B* with 20 µm sealing ring, compared to the package of *Configuration II-A* with the same sealing ring width (3.8×10^{-11} and 8.7×10^{-14} mbar.l/s). This reduction in leak rates comes despite the fact that the package of *Configuration II-B* is 31% larger in area and 14% larger in circumference—and therefore susceptible to more leakage—than the packages of *Configuration II-A*. Another interesting observation is that lateral extension and increased thickness of the nitride sealing layer lead to more reduction in air leakage (almost 2 orders of magnitude) compared to the reduction in He leakage (approximately one order of magnitude). This can be explained by the larger size of air molecules which tend to leak into the packages through larger channels at the package edges rather than permeate through the cap layers (which is a more dominant transfer mechanism in the case of He).

A large difference (typically more than two orders of magnitude) is further observed in the obtained standard leak rates between the He leak test and the air leak test for each package. This can be attributed to the different leakage paths (or mechanisms) available for gas molecules of different sizes. The smaller helium molecules feature a higher permeation capability through the cap membrane and easier flow through smaller interface defects in comparison to the larger air molecules like nitrogen or oxygen. The physical difference between He and air molecules is partially considered by the molar mass ratio in equation (4.2). However, the results in Fig. 4.7 suggest that the molar mass ratio is not a sufficient description of the actual difference between He and air in terms of leakage properties in such thin film packages.

The results in Fig. 4.7 show the error range of the obtained standard leak rate values which is based on an estimated error of ± 50 nm in the cap deflection measurements. Depending on the package dimensions, the test duration, the gas and pressure used, this estimated cap deformation error can be translated to an error range in the obtained leak rate using equations (4.1 to 4.3). As mentioned earlier, this error range includes the uncertainties caused by the cap surface roughness and the finite precision of the optical interferometry measurement. According to the lowest obtained leak rate values for the package of *Configuration I-B*, the presented hermeticity testing

method is capable of detecting standard leak rates as low as 10^{-14} mbar.l/s for a short term He leak test and 5×10^{-16} mbar.l/s for a long term air leak test.

In order to evaluate the impact of the leak rates discussed above on the package performance in practical applications, we can calculate the internal package pressure increase in air after sealing by rewriting equation (4.2) as follows:

$$\Delta P = P_1\left(1 - e^{-L_s \Delta t / V P_0}\right) \tag{4.4}$$

where P_1 is the partial differential pressure of air across the cap at the beginning of the package lifetime, L_s is the standard leak rate in air (as reported for different package configurations in Fig. 4.7), V is the internal cavity volume, P_0 is the atmospheric pressure (1 bar) and Δt is the time encountered by the package under atmospheric conditions.

Equation (4.4) is used to obtain the pressure evolution curves shown in Fig. 4.8 for a typical micropackage of 1 nl internal volume (corresponding to cavity dimensions of $500 \times 500 \times 4$ μm^3). Here the increase in the internal package pressure (which is assumed to be initially very low, or <0.01 mbar) is shown over a period of 10 years assuming standard air leak rates in the range of 10^{-13} mbar.l/s to 10^{-16} mbar.l/s (corresponding to the results in Fig. 4.7). The actual compatibility of the thin film package with a specific application depends on the requirements of the encapsulated microsystem and the properties of the 1-level packaging technique used. On the one hand, a thin film package with leak rate in the range of 10^{-15} to 10^{-16} mbar.l/s in combination with a low-cost (non-hermetic) 1-level package can be the proper choice for MEMS devices, such as accelerometers or capacitive switches that require only a clean (or dry) operational environment. On the other hand, a hermetic 1-level package in addition to the temporary protection of the thin film package (for 1 to 10 days) is more suitable for devices such as MEMS gyroscopes and high-Q microresonators that require a very low operating pressure (< 0.1 mbar). Finally, packages with air leak rates around 10^{-14} mbar.l/s or above would lead to a saturation of the cavity with air within the suggested lifetime of 10 years. This kind of micropackages is therefore only useful in combination with more hermetic 1-level packaging or in application that do not require full isolation from the surrounding environment.

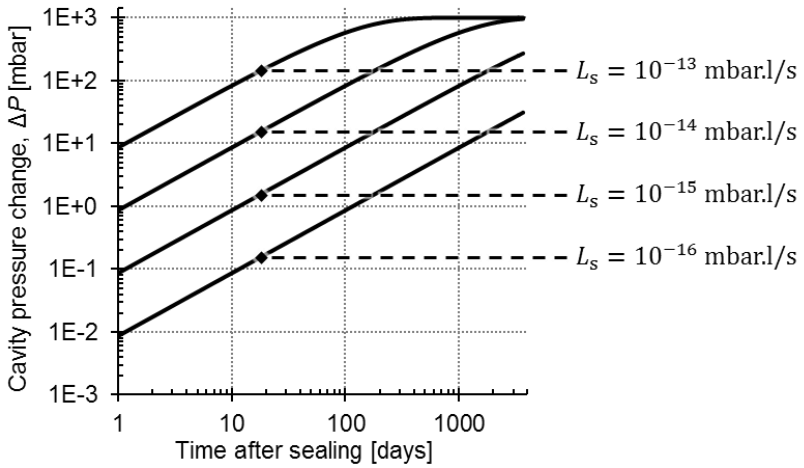


Fig. 4.8 The calculated internal pressure increase for a vacuum-sealed package of 1 nl internal volume, exposed to an external atmospheric pressure for a period of 3650 days (=10 years), for different values of standard air leak rate (L_s).

4.3 Pressure monitoring using microsensors

The helium and air leak tests based on cap deformation provide a relatively accurate assessment of the hermeticity of the micropackages as discussed above. However, this cap deformation method provides little information about the actual pressure inside the micropackages after being sealed. This information can be vital for microsystems that require a very low pressure for proper operation (see Table 1.1). By knowing the sealing process conditions, one can estimate the internal pressure and gas composition of the package immediately after sealing using the ideal gas law as discussed earlier in Chapter 2. However, the actual pressure and gas composition can be rather different if significant leakages or outgassing take place after the sealing process; hence the need for embedded microsensors to monitor the internal pressure of the micropackages. In the following subsections, the results of an experimental investigation of two kinds of Ni-based microsensors that can be used to monitor the internal pressure of the micropackages are discussed. These microsensors have not been used to monitor the actual pressure inside the PAA-based micropackages discussed in this work but they are presented here as a viable solution for future experiments where such internal pressure monitoring is needed.

4.3.1 Nickel-based microresonators

It has been established that the quality factor (Q-factor) of microresonators is dependent on the surrounding pressure (Blom *et al*., 1992; De Coster *et al*., 2005). Typically, a decrease in the Q-factor of a microresonator is observed when the surrounding pressure increases. This is mainly due to the motion damping through collision between the microresonator and the surrounding gas molecules (see Fig. 4.9(a)). These collisions take place at the surface of the microresonator; hence the resulting motion damping (or sensitivity to pressure) depends on the geometry of the microresonator.

As discussed in Chapter 2, Ni-based MEMS have been fabricated in order to investigate their compatibility with the PAA-based thin film packaging technology (as in Fig. 2.22). Among the devices that have been realized are Ni-based microresonators intended as encapsulated pressure sensors as shown in Fig. 4.9. These are planar Ni-based microstructures of approximately 2.3 μm thickness. Al-based electrodes underneath the freestanding microresonators facilitate their electrostatic actuation through a vertical gap of approximately 2 μm height as illustrated in Fig. 4.9(a). Moreover, release holes are defined in the resonating structures to facilitate the release-etching of the sacrificial layer to form this vertical gap and enable the vertical motion of the microresonators. The first type of microresonators is a traditional rectangular beam with fixed ends as shown in Fig. 4.9(b). Another type of microresonators features a relatively large disk of Ni which is anchored at four uniformly distributed points using small cantilever-shaped beams as shown in Fig. 4.9(c). This microresonator has been designed in this manner to have a relatively large surface area—allowing for more interaction with the surrounding ambient and potentially higher sensitivity to pressure changes.

In order to use such Ni microresonators for pressure sensing, one needs to evaluate their dynamic response within a certain frequency range around their natural vibration frequency. This frequency is typically dependent on the microresonator geometry, material, mechanical support and loading. It has been shown that the first natural vibration frequency (f_0) of a wide beam with a rectangular cross-section and fixed ends (as in Fig. 4.9(a,b)) can be calculated using the formula (Tilmans *et al.*, 1992):

$$f_0 = \frac{{a_1}^2\, t}{2\pi\sqrt{12}\, l^2} \sqrt{\frac{E}{12\,\rho(1-\nu^2)}} \sqrt{1 + b_1 \frac{\sigma}{E}(1-\nu^2)\left(\frac{l}{t}\right)^2} \qquad (4.4)$$

where t is the beam thickness, l is the beam length, E is Young's modulus (195 GPa for electroplated Ni, according to Majjad *et al.* (1999)), ρ is the mass density (8900 kg/m^3 for Ni), ν is Poisson's ratio (typically 0.3 for metals), σ is the axial tensile stress in the beam, and finally a_1 and b_1 are constants determined by the shape of the vibration mode. For the first vibration mode of the rectangular beam, it has been shown that $a_1 = 4.730$ and $b_1 = 0.295$ (Tilmans *et al.*, 1992). For a Ni beam of 2.3 μm thickness and 300 μm length with fixed ends, as in Fig. 4.9(b), equation (4.4) yields a resonance frequency of 129 kHz assuming the beam is stress-free ($\sigma = 0$). However, the measured resonance frequency of this structure was found to be 344 kHz. This higher measured resonance frequency can be attributed to a tensile stress in the beam which was caused by annealing it a relatively high temperature close to 250 °C before releasing it (see Fig. 2.21). Using equation (4.4), a tensile stress (σ) value of 262 MPa was found to correspond to the measured resonance frequency of 344 kHz for this specific rectangular beam.

For the disk-shaped microresonator shown in Fig. 4.9(c), the natural frequency can be estimated by considering the disk as a mass suspended by four small cantilever springs with a guided end at the side of the disk. The mass of the Ni disk can be approximated to that of a cylinder of a similar shape ($m = \rho V = \rho\pi d^2 t/4$; where d is the disk diameter). The spring constant (k) of a cantilever of width w and length l (with one fixed end and the other end guided) can be obtained using the formula: $k = Ewt^3/l^3$ (Young and Budynas, 2002). Hence, the first natural vibration frequency of the disk microresonator supported by 4 small cantilevers can be estimated by using the principle of simple harmonic oscillation as follows:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}} = \frac{t}{d}\sqrt{\frac{E\,(4w)}{\pi^3\, l^3 \rho}} \tag{4.5}$$

For a disk microresonator of 540 μm diameter (d) with 4 springs of 30 μm length (l) and 4 μm width each (w), as in Fig. 4.9(c), equation (4.5) yields a resonance frequency of 87 kHz. The measured resonance frequency of this structure was found to be close to 68 kHz. The difference between the measured and calculated resonance frequencies is potentially caused by small differences in the geometrical parameters or material properties of the fabricated Ni microstructures, compared to the theoretical values used in the model.

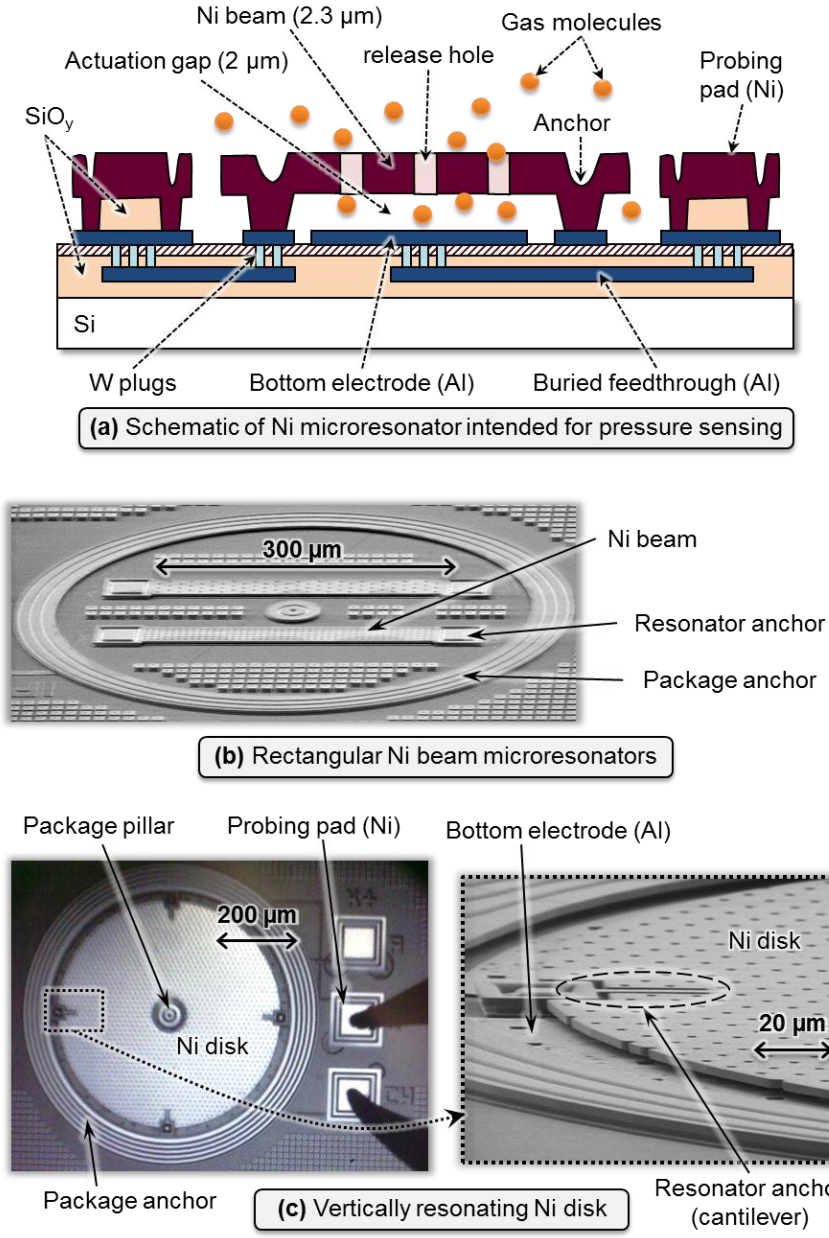


Fig. 4.9 (a) Cross-sectional schematic; and (b,c) micrographs showing Ni-based microresonators intended to monitor the pressure inside a micropackage (only the anchor of the package is shown). These microstructures are realized using the Ni MEMS technology described in Chapter 2 (as in Fig. 2.22).

One way to (electrostatically) measure the Q-factor of a microresonator is by applying a DC bias between the resonator and the bottom electrode; forming a charged capacitance. Then a small AC signal with varying frequency is applied to this 1-port circuit between the resonator and the bottom electrode. Near its resonance frequency, the microresonator vibrates in response to the alternating electrostatic attraction, causing an increase in the flowing AC current due to the oscillating capacitance of the system (Tilmans *et al.*, 1992). This electromechanical resonance behavior can be observed on the measured conductance as a function of frequency as in Fig. 4.10(a).

By increasing the surrounding pressure, damping of the resonance increases as seen in Fig. 4.10(a). The Q-factor (a good measure of the motion damping) can be obtained using the formula: $Q = f_0/\Delta f$; where f_0 can be defined as the frequency corresponding to maximum conductance (G_{Emax}). Δf is the bandwidth of the resonance which can be defined as the frequency range in which the conductance is higher than $G_{\mathrm{Emax}}/2$ (or where the transmitted power is within a 3 dB range of the maximum power).

By repeating the frequency response measurements for different microresonators at different surrounding nitrogen pressures, the results in Fig. 4.10(b) are obtained. Generally speaking, these results show an exponential Q-factor reduction in all three microresonators for pressures above 0.5 mbar. Some configurations like the disk microresonator of 340 µm diameter show a relatively high and stable Q-factor sensitivity to pressure within a certain pressure range (0.5 to 5.0 mbar). It is worth mentioning that at higher pressure values (>10 mbar) it was challenging to obtain the Q-factor (or identify the resonance region) from the measured conductance characteristics of the microresonators. This is mainly attributed to the relatively low amplitude of oscillation at higher pressures due to the increasing mechanical losses (for instance, due to squeeze film damping (Andrews *et al.*, 1993)). This limited range of pressures (from 0.5 to 10 mbar) that can be detected by the microresonators makes them less practical in monitoring the internal package pressure if the initial sealing pressure or the final pressure (after leakage or outgassing) fall outside this small range.

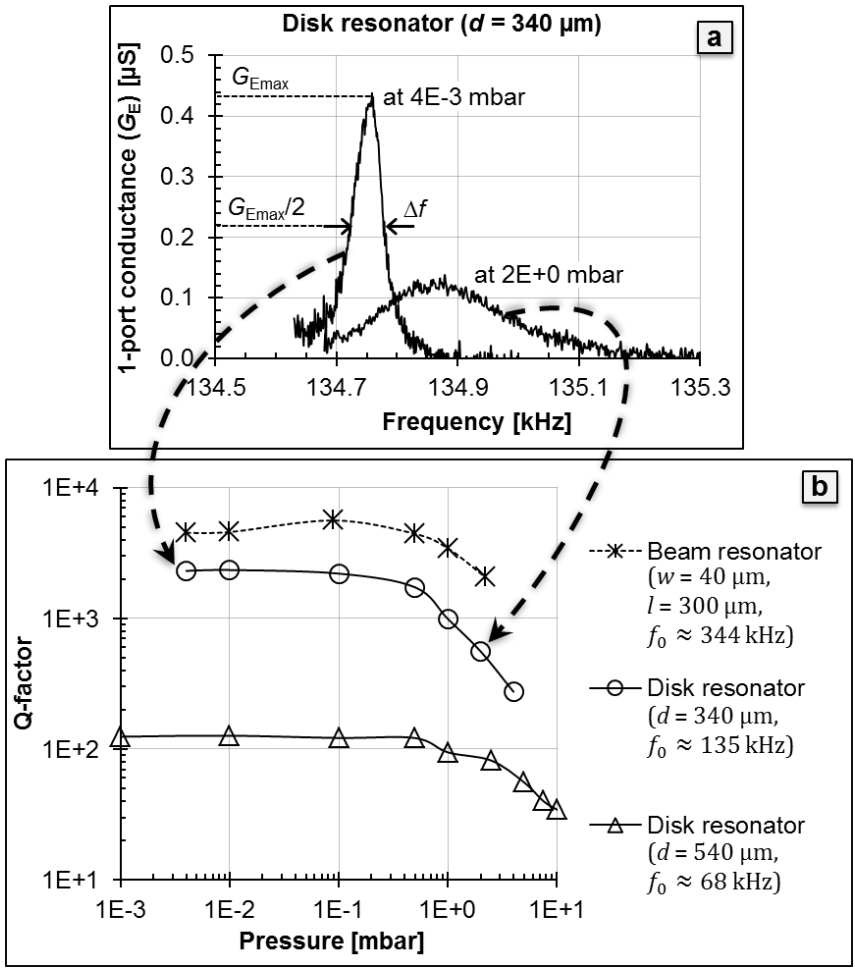


Fig. 4.10 (a) The measured 1-port conductance vs. frequency curves used to obtain the Q-factor of a disk resonator at 2 different pressures; and (b) the measured change in Q-factor vs. the surrounding nitrogen pressure for three different microresonators.

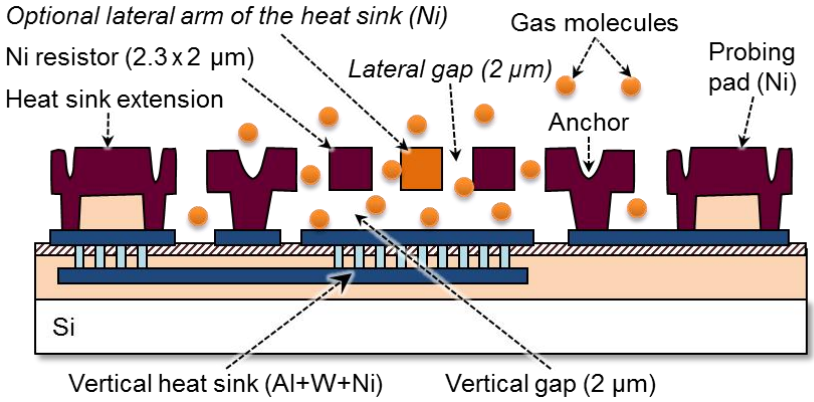
4.3.2 Nickel-based micro-Pirani gauges

Nickel is traditionally a good candidate to build Pirani gauges which can measure pressure changes indirectly by sensing the change in thermal conduction of their surrounding medium (Ellett and Zabel, 1931). This is typically done by measuring the resistance of a thin wire of nickel in close proximity to a heat sink. The resistance of the wire is dependent on its temperature which is in turn dependent on the amount of heat generated in

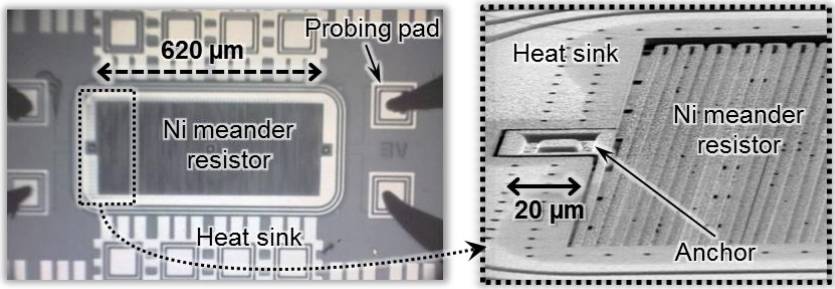
the wire (by Joule heating) as well as the amount of heat lost by gaseous conduction. An increase in the gas pressure would lead to an increase in the heat lost from the wire (to the heat sink) by conduction, and therefore the wire temperature (and resistance) would decrease. In order to localize the pressure measurement, a 4-wire (Kelvin) circuit is used to eliminate the effect of resistance changes other than the actual wire resistance.

Micro-Pirani gauges (based on thin Ni meander resistors) have been implemented as shown in Fig. 4.11 using the Ni MEMS technology described in Chapter 2. The Ni wire of the meander resistor is typically 2 μm wide, 2.3 μm thick and covers an area of 620 × 250 μm^2 (total wire length is up to 20 mm). The heat sink of the gauges is constructed as a large area of interconnected Ni and Al layers. In one configuration, the heat sink is brought in proximity with the Pirani gauges using the underlying (bottom electrode) Al layer through a vertical gap of 2 μm height, as shown in Fig. 4.11(a,b). In another configuration, additional lateral arms of the heat sink are extended between the meander resistor sections (with a lateral gap of approximately 2 μm) as shown in Fig. 4.11(a,c). This latter configuration is expected enhance the sensitivity of the Pirani gauge to pressure variations by increasing the portion of the resistor surface area in proximity with the heat sink (Chae *et al.*, 2005).

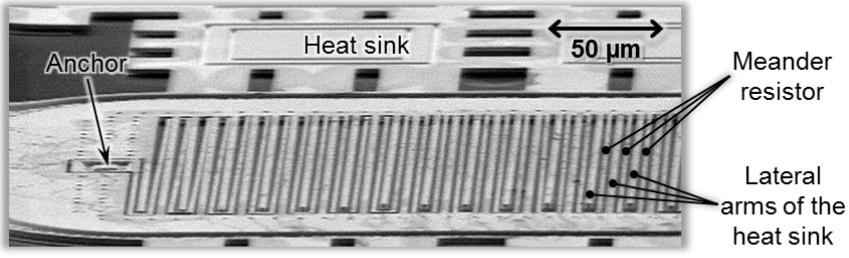
The gauge resistance has been measured while changing the surrounding nitrogen pressure in a sealed chamber, yielding the results in Fig. 4.12. These results indicate a higher sensitivity for the Pirani gauge with both vertical- and lateral-gap heat exchanges (as expected thanks to the better proximity of the meander resistor and the heat sink). Moreover, the dynamic pressure range of both Pirani gauges (from 0.1 mbar up to 100 mbar) is larger than the dynamic range of the microresonators discussed earlier. However, it has been observed that a certain settling time (from few seconds to few minutes) is needed to reach a stable resistance value when the surrounding pressure changes. This can be attributed to either a slow heat exchange at lower pressures (the number of gas molecule collisions decrease at lower pressures), or a noise effect caused by the heat circulation through the measurement setup at high pressures (the large probing needles can act as an extra heat sink and conduction path; see Fig. 4.11(b)). Generally speaking, the micro-Pirani gauges are less accurate in detecting fast changes in pressure. However, their large dynamic pressure range makes them more suited for long-term pressure monitoring (for fine leak testing) if needed.



(a) Schematic cross-section of Ni-based micro-Pirani gauge



(b) Ni micro-Pirani gauge with vertical heat sink only



(c) Ni micro-Pirani gauge with vertical and *lateral* heat sink

Fig. 4.11 (a) Cross-sectional schematic and (b,c) micrographs showing two different types of Ni-based micro-Pirani gauges. In (b) the Ni resistor can dissipate heat through a vertical gap only; while in (c) lateral arms of the heat sink are added. These microstructures are realized using the Ni MEMS technology described in Chapter 2 (as in Fig. 2.22).

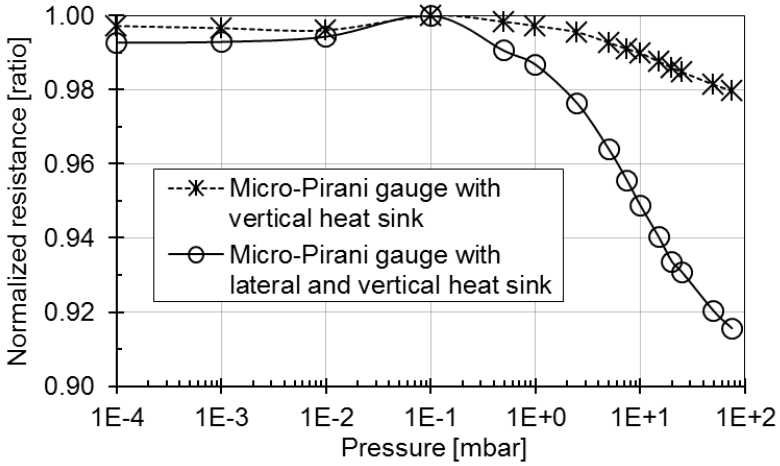


Fig. 4.12 Normalized resistance variation vs. the surrounding nitrogen pressure for the two different micro-Pirani gauge configurations shown in Fig. 4.11.

4.4 Reliability assessment

Microsystems chips can be exposed to rather extreme stresses during their fabrication, storage and operation. Consider as a simple example the extreme temperature variations in outer space applications where temperatures can vary between –100 °C and +120 °C depending on the amount of sun light captured by an object. A micropackage intended for such applications should in turn withstand the impact of these environmental changes. In order to evaluate the resistance of PAA-based micropackages to extreme environmental conditions, four chips with empty micropackages of *Configuration I-B* (with lateral cap dimensions in the range of 350 to 500 µm, sealed with a 4 µm-thick SiN_z layer, as in Fig. 2.14(b)) have been submitted to different reliability tests as listed in Table 4.2. The test conditions used are based on the commonly employed JEDEC standards for the testing of microelectronic chips. An optical gross leak test (as described in section 4.2.1) is applied to each package before and after the reliability stress to identify packages that undergo significant damage during the stress test. A thin Ti layer (30 nm) is deposited on the samples to provide sufficient optical reflection for the gross leak test. A micropackage is considered air-tight if it shows a deformation larger than 50% of the expected value (based on an analytical deflection model) due to an ambient pressure change of 0.8 bar (as in Fig. 4.2 and Fig. 4.3). The outcome of this optical gross leak test is then used

to estimate the survival rate of the thin film packages under the applied thermomechanical or environmental stresses.

According to the results in Table 4.2, the micropackages can withstand repeated mechanical shocks of 200 *g* amplitude and 1.5 ms duration (shock test) without significant damage that would impact their air-tightness. Similarly, a large number of the micropackages survived extreme temperature cycling between –40 °C and +150 °C (250 consecutive cycles of one hour each). Exposure to high humidity and high temperature levels (85% RH at +85 °C) for a period of 250 hours is also proven to be an extreme stress that the micropackages can withstand without encountering large leakages. The most extreme reliability stress test applied to the micropackages is the pressure cooker test with exposure to 100% RH (or 2 bar of water vapor pressure) at +121 °C. In this case, it was observed that the thin Ti layer used to enhance the optical reflectivity of the thin caps was partially damaged during the test. This resulted in the disqualification of potentially intact packages in the final gross leak test after the pressure cooker stress test due to the Ti layer instability (see Fig. 4.13). Therefore, the actual resistance of the thin film packages to the pressure cooker test can be higher than indicated by the 69% survival rate given in Table 4.2.

Table 4.2 Summary of four reliability stress tests applied to micropackages of *Configuration I-B* (as in Fig. 2.14(b)).

Reliability test	Related JEDEC standard	Number of packages with no gross leak		Survival rate (for air-tightness)
		Before	After	
Shock test: 10 successive acceleration pulses of 200 *g* amplitude and 1.5 ms duration.	JESD22-B111	31	31	100%
Temperature cycling: 250 cycles between –40 °C and +150 °C (1 hour per cycle).	JESD22-A104	26	26	100%
85/85 test: 250 hours exposure to +85 °C and 85% RH (0.5 bar vapor pressure).	JESD22-A101	20	20	100%
Pressure cooker: 96 hours exposure to +121 °C and 100% RH (2 bar vapor pressure).	JESD22-A102	16	11	69%

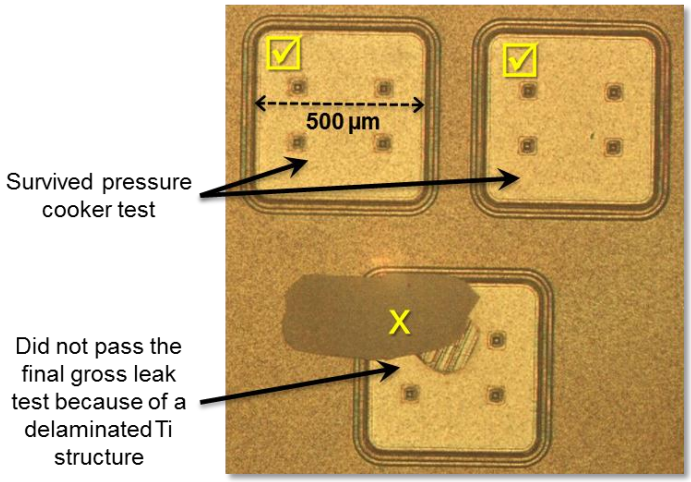


Fig. 4.13 Micrograph of three thin film packages after being submitted to the pressure cooker reliability test described in Table 4.2.

4.5 Conclusions

Several phenomena such as leakage and outgassing can lead to a degradation of the internal environment of a micropackage. It is therefore necessary to evaluate the hermeticity of thin film packages for applications that require a stable low pressure (vacuum) for proper operation of the encapsulated microsystem. Using a simple and rather accurate hermeticity test based on cap deformation, it has been shown that widening the package sealing ring from 10 µm up to 30 µm reduces both helium and air leak rates by more than an order of magnitude. When the thin film interfaces at the package edge are eliminated (as in *Configuration I*), very low leak rates close to 5×10^{-15} mbar.l/s for He and 1×10^{-16} mbar.l/s for air are obtained. Moreover, it has been shown that Ni-based microsensors such as microresonators and micro-Pirani gauges can be used to monitor the evolution of the internal package pressure if needed. Reaching a high level of micropackage hermeticity paves the way for a wide range of microsystems to be used in different applications. Finally, the thin film packages fabricated using nanoporous alumina reveal rather high survival rates (69% to 100% of the micropackages remain air-tight) when subjected to extreme thermomechanical and environmental stresses including repeated exposure to accelerations up to 200 *g*, cycling between temperatures down to –40 °C and up to +150 °C, as well as exposure to extreme humidity (water vapor pressures up to 2 bar at +121 °C).

Chapter 5 Compatibility with RF microsystems

In this chapter, the compatibility of the encapsulation technology based on nanoporous alumina with RF microsystems is investigated. First, the design principles of a coplanar waveguide that can deliver high frequency signals across the boundaries of the micropackages are discussed. Electromagnetic simulations are further used to validate the design principle and assess the expected performance. Finally, an experimental investigation is presented where the RF performance of encapsulated transmission lines is measured and compared to an unpackaged (reference) transmission line.

5.1 RF feedthrough design for PAA-based micropackages

In radio frequency (RF) microsystems, high frequency (1-80 GHz) signals are typically routed on-chip by means of planar transmission lines (TL's) such as coplanar waveguides (CPW's). The RF characteristics of such TL's are essential in determining the overall performance of the system. Ideally the transmission line should not introduce any losses to the system (insertion loss is zero and no reflection). The TL delivering an RF signal to or from an encapsulated microsystem interacts with the micropackage and should therefore be designed to minimize the added signal losses due to this interaction. In order to achieve this goal, only dielectric materials of low RF loss should be used to construct the cap of the micropackage. It is known from existing literature that both nanoporous alumina (PAA) and PECVD SiN_z

satisfy this condition (He and Kim, 2009; Detcheverry *et al.*, 2004). However, the package anchor (or sealing ring) includes a small portion of Al which is believed to be essential for the mechanical stability and hermeticity of the package. This conductive portion of the sealing ring is typically connected to the electrical ground because of its large overlap with the ground plates of the encapsulated RF line as shown in Fig. 5.1. At the package edge, the grounded sealing ring is capacitively coupled through a 1 μm-thick dielectric stack of silicon oxide (0.6 μm) and silicon carbide (0.4 μm) to the underlying (buried) signal line (0.9 μm-thick Al layer); thus locally forming a microstrip line (MSL). This capacitive coupling of the MSL configuration can cause undesired reflections to the RF signal in the buried feedthrough, in addition to losses in the transmitted signal power due to the signal leakage into the ground.

For the encapsulated transmission line shown in Fig. 5.1, the CPW outside the micropackage is coupled to a similar CPW inside the package through the buried feedthrough which has a finite resistance, capacitance (through coupling to the grounded sealing ring) and inductance. On the one hand, a small buried feedthrough resistance (R_b)—and hence a large feedthrough width (w_b)—is desired to minimize any resistive losses to the RF signal. On the other hand, a small feedthrough capacitance (C_b)—and hence a small feedthrough width (w_b)—is desired to minimize the signal coupling (or leakage) to the ground. This apparent contradiction in the impact of w_b on the final RF characteristics necessitates a detailed analysis to reach the best compromise (optimum design). Moreover, the equivalent inductance of the feedthrough (L_b), which is dependent on its length (l_{bf}), is another crucial element that determines the characteristic impedance of the feedthrough. A good impedance matching between the buried feedthrough and the CPW is important to reduce any undesired signal reflections at the TL transition at the package edge.

Furthermore, other design parameters like the sealing ring width (w_S) can influence the RF characteristics of the structure (note that $C_b = \varepsilon_d w_b w_S / t_d$; where ε_d is the equivalent permittivity of the SiO_y+SiC dielectric stack and t_d is its thickness). However, this sealing ring width has a significant impact on the hermeticity of the micropackage (as discussed in Chapter 3Chapter 4) and should therefore not be smaller than a typical value of 20 μm. Although the simplified circuit model in Fig. 5.1(c) provides a basic understanding of the buried feedthrough behavior, a more extensive model is needed to accurately simulate the propagation of electromagnetic waves (at high frequencies) through the complex (3D) structure of the encapsulated CPW, and hence gain more understanding and reach an optimum design.

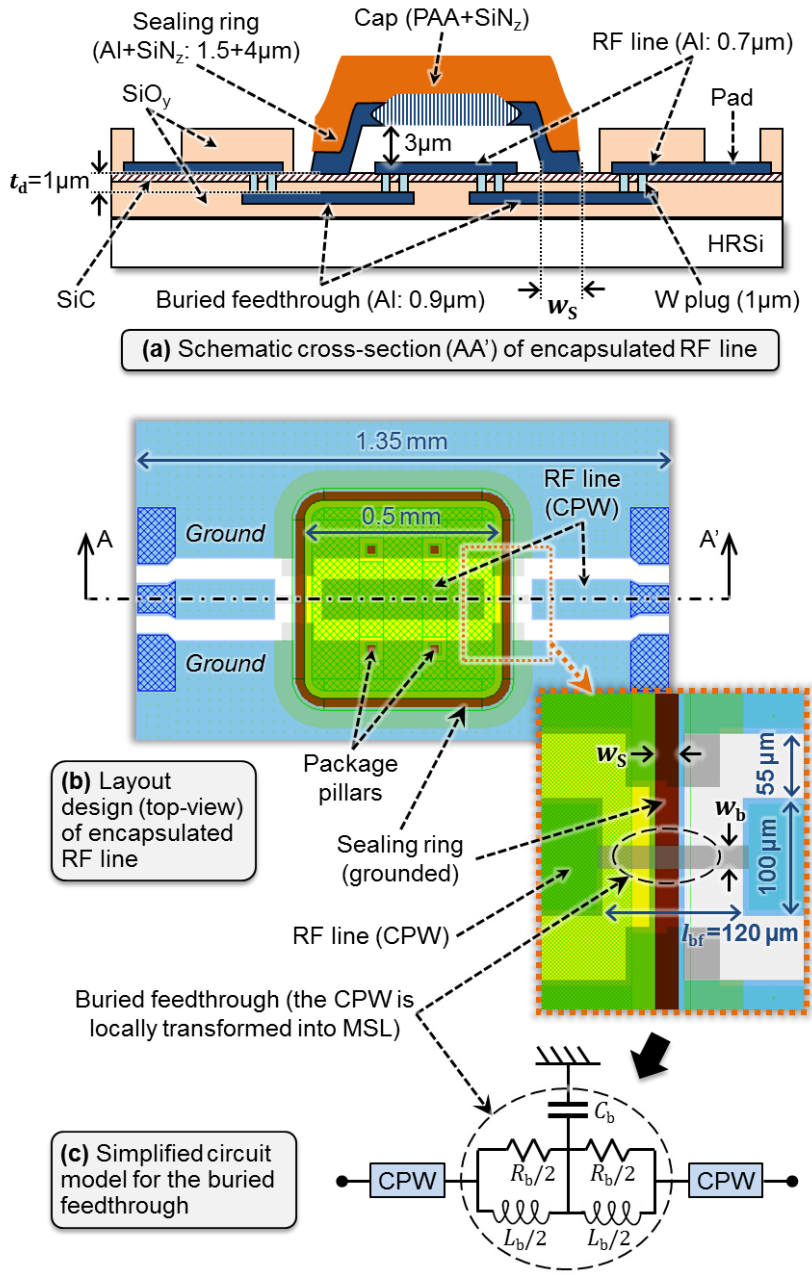


Fig. 5.1 (a,b) Cross-sectional schematic and layout design (top-view) of an encapsulated RF transmission line (CPW); and (c) simplified circuit model for the TL transition through the package anchor.

A 3D finite element electromagnetic model was built using Ansoft HFSS software in order to perform a simulation-based study of the RF characteristics of the encapsulated transmission line shown in Fig. 5.1. This was done in collaboration with researchers from the University of Perugia in Italy, in the frame of MEMSPACK project (www.memspack.eu). The main materials and dimensions used in this model are shown in Fig. 5.1 (the substrate used is 0.7 mm-thick HRSi with a resistivity of 2.0 kΩ.cm). Such FEM simulations produced frequency-dependent S-parameters of the encapsulated TL as shown in Fig. 5.2. The results in Fig. 5.2(a,b) illustrate the significant performance enhancement achieved by locally reducing the buried feedthrough width (w_b) underneath the sealing ring. A substantial reduction in the undesired signal reflection ($|S_{11}|$) is achieved for a wide frequency range by decreasing w_b from 100 μm (the original CPW width) to 20 μm. This is mainly attributed to a better impedance matching between the CPW (50 Ω characteristic impedance) and the buried feedthrough with 20 μm width (its length is 120 μm as shown in Fig. 5.1(b)). Similarly, an overall reduction in the insertion loss (or an enhancement in the transmission ratio: $|S_{12}|$) is obtained by narrowing of the buried feedthrough. This improvement is the result of reducing the coupling capacitance (C_b) between the buried feedthrough and the sealing ring (less leakage of the RF signal to the ground). Further reduction of the feedthrough width (<20 μm) was found to provide no improvement in terms of insertion loss because of the increasing resistance of the narrow feedthrough. This reduction in the feedthrough width is also undesired because it compromises the reliability of the transmission line (due to joule heating) when RF signals of relatively high power are involved. Note that the DC resistance of one buried feedthrough of 20 μm width is around 0.2 Ω (assuming the Al thin film resistivity is around 3 μΩ.cm).

Another example of the FEM simulation results is shown in 5.2(c,d)**Error! eference source not found.**. Here the buried feedthrough width (w_b) is fixed at 20 μm, while the sealing ring width (w_S) is changed from 20 to 50 μm. Such widening of the sealing ring can be useful in enhancing the hermeticity of the thin film packages as discussed earlier in Chapter 4. The simulation results show a minor impact of the sealing ring widening on the RF characteristics of the transmission line. Both the transmission ratio ($|S_{12}|$) and the return loss ($|S_{11}|$) remain at comparable levels throughout the frequency range of 0 to 50 GHz, except for an increase in return loss between 25 and 40 GHz with a wider sealing ring. The reason why this relatively big change in the sealing ring width has a minor impact on the RF characteristics is related to the value of the buried feedthrough width (w_b). In this specific case, w_b is relatively small (20 μm) and therefore it has the most dominant impact on the insertion

loss due to its high resistance. As mentioned earlier, the return loss (which is mainly determined by the impedance matching between the feedthrough and the CPW) is slightly impacted by widening the sealing ring due to the change in the capacitance between the feedthrough and the sealing ring (C_b as in Fig. 5.1).

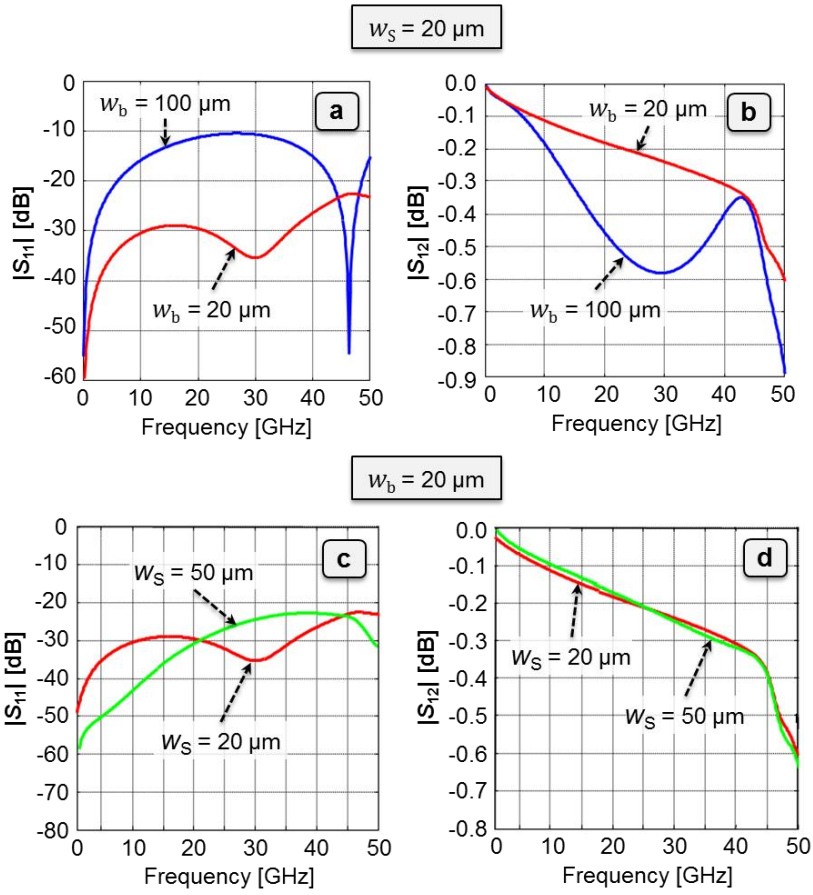


Fig. 5.2 Electromagnetic simulation results of a 1.35 mm-long 2-port CPW, partially encapsulated by a thin film package of (as in Fig. 5.1): (a,b) The return loss ($|S_{11}|$) and the transmission ratio ($|S_{12}|$) for two configurations of the buried feedthrough width (w_b) at a fixed sealing ring width (w_S); (c,d) The return loss ($|S_{11}|$) and the transmission ratio ($|S_{12}|$) for two configurations of the sealing ring width (w_S) at a fixed buried feedthrough width (w_b).

5.2 Characterization of encapsulated RF lines

The improved feedthrough design described above has been validated by fabricating and characterizing the three test structures shown in Fig. 5.3: **(a)** unpackaged or reference CPW with 100 µm-wide signal line; **(b)** full width (100 µm) CPW which is partially encapsulated with a thin film package; and **(c)** partially encapsulated CPW with a reduced buried feedthrough width of 20 µm (with the same package structure). All three structures have been fabricated on the same HRSi substrate (200 mm wafer) using the packaged RF line technology described earlier in Chapter 2 (*Configuration II-A*, as in Fig. 2.16, Fig. 2.18 and Fig. 2.19). The thin film packages shown in Fig. 5.3(b,c) have lateral dimensions of 0.5×0.5 mm^2 and a sealing ring width of 20 µm.

The RF characterization results shown in Fig. 5.4 essentially validate the design recommendation indicated earlier (a significant improvement in RF performance is obtained by narrowing the buried feedthrough to 20 µm). In terms of insertion loss (or transmission ratio: $|S_{12}|$), the results in Fig. 5.4(a) show a similar performance for the packaged CPW with narrow feedthroughs ($w_b = 20$ µm) as compared to the reference CPW. Given that the main cause of the insertion loss for the reference CPW is the partial conduction of the HRSi substrate, this indicates that the added loss of the two narrow feedthroughs (due to the Al resistance and capacitive coupling with the sealing ring) is rather insignificant in this case. Moreover, the packaged CPW with normal feedthrough width ($w_b = 100$ µm) exhibits a higher insertion loss than the other two structures. This is caused by the additional capacitive coupling between the (wide) feedthrough and the sealing ring, leading to signal leakage to the grounded sealing ring. This effect becomes rather dominant at relatively high frequencies (>40 GHz) because the impedance of this capacitive coupling path is inversely proportional to the frequency.

The results in Fig. 5.4(b) further show a comparison between the frequency-dependent return loss ($|S_{11}|$) for the three TL's shown in Fig. 5.3. Here a slightly better performance (lower return loss) is observed for the packaged CPW with narrow feedthroughs ($w_b = 20$ µm) compared to the reference CPW (for frequencies up to 60 GHz). This can be explained by a better impedance matching between the packaged CPW (with $w_b = 20$ µm) and the measurement system (an RF network analyzer with on-wafer probes), compared to the reference CPW. Furthermore, the higher capacitance between the sealing ring and the CPW with normal feedthrough width ($w_b = 100$ µm) causes a clear degradation in return loss for this packaged

CPW. These results are in agreement with the simulation-based results discussed earlier (compare Fig. 5.2(a,b) and Fig. 5.4).

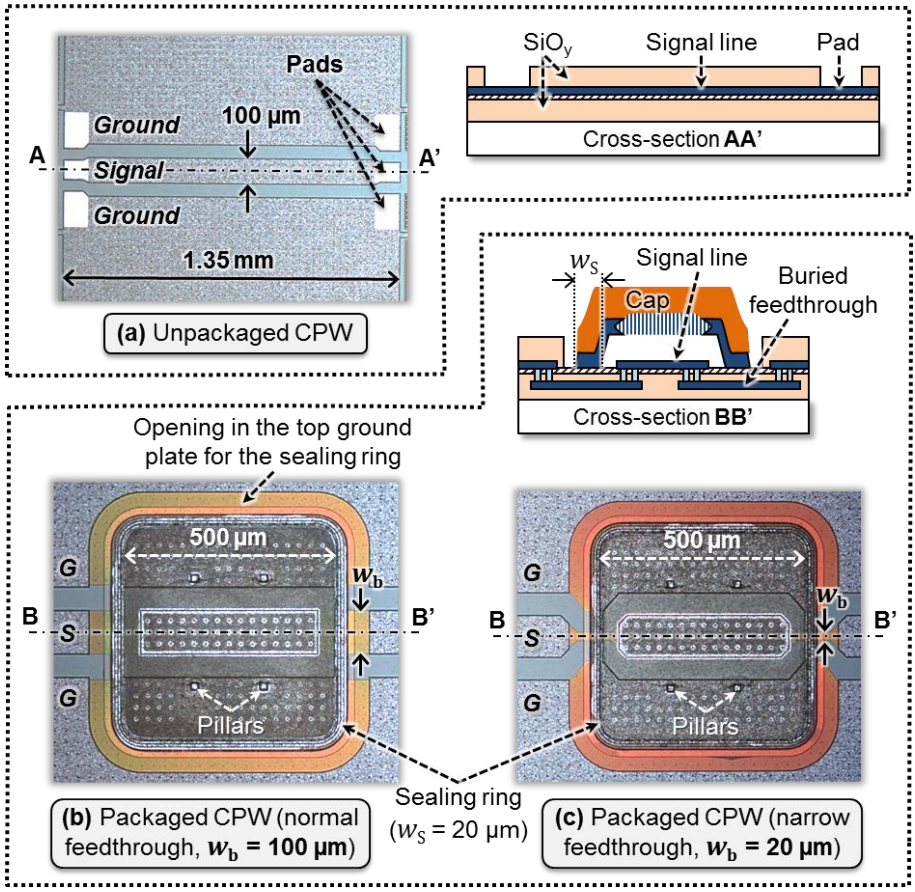


Fig. 5.3 Top-view micrographs and cross-sectional schematics of: (a) an unpackaged (reference) CPW; (b) a packaged CPW with normal buried feedthrough width (100 µm); and (c) a packaged CPW with reduced buried feedthrough width (20 µm). In all 3 cases the total length of the Al-based transmission line is 1.35 mm and the substrate is HRSi.

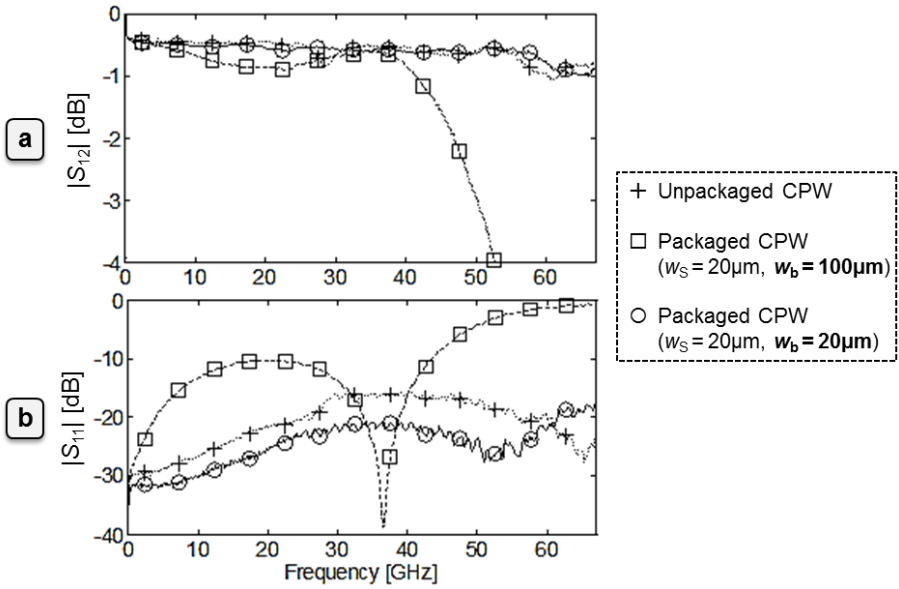


Fig. 5.4 Measured RF characteristics of the three transmission lines shown in Fig. 5.3: (a) transmission ratio ($|S_{12}|$); and (b) return loss ($|S_{11}|$). All 3 transmission lines are 1.35 mm in length (*i.e.*, the distance between the reference planes for the S-parameter measurements).

5.3 Conclusions

To enhance the compatibility of the thin film packages (based on nanoporous alumina) with RF microsystems, a specially configured coplanar waveguide (CPW) has been designed, implemented and tested. In this special CPW, the width of the buried feedthrough delivering the RF signals across the package anchor (sealing ring) is reduced from the original signal line width of 100 µm to an improved design of 20 µm. The resulting RF performance of the encapsulated CPW with the improved feedthrough design is comparable to that of an unpackaged (reference) CPW with full signal line width up to the maximum frequency used in the RF measurements (67 GHz). This proves the compatibility of the encapsulation technology based on nanoporous alumina (including an Al-based sealing ring) with RF microsystems in a wide frequency range.

Chapter 6 Conclusions and future work

This chapter provides an overview of the innovative solutions presented in this thesis for the technological, design and testing challenges related to microsystems encapsulation using nanoporous alumina. Additionally, a number of relevant technological and design-related challenges that require further investigation are discussed. Finally, the potential of nanoporous alumina as a microsystems material is highlighted by a few examples of new concepts and applications that can utilize the distinct features of this material.

6.1 Main achievements of this work

6.1.1 Technological innovations

Innovative and simple surface micromachining processes and integration schemes have been a key aim and enabler in this pursuit of an effective encapsulation method for microsystems. This research started by revisiting the critical process of producing freestanding thin membranes of nanoporous alumina (or PAA)—considered at the beginning of this work as a complex and unstable process. Months of research and experimentation resulted in developing the first anodization process that produces fully permeable nanoporous alumina membranes in a single fabrication step. Neither seed layers nor a separate alumina etching step are needed in this new method. Moreover, large numbers of freestanding membranes of nanoporous alumina were produced for the first time on large substrates (200 mm wafers) in a true batch-processing fashion. This was further facilitated by a new design

concept for the photoresist mask of the anodization process. The final result is a simple, scalable and self-limiting anodization process that is rather insensitive to non-uniformities of thin films on large substrates. Moreover, the new anodization process is relatively cost-effective in a volume manufacturing environment, as it typically lasts less than 30 minutes and can be applied to a full batch of wafers in parallel. The produced nanoporous alumina membranes are typically 1.5 to 3 μm in thickness and feature cylindrical nanopores of 10 to 20 nm diameters and pore-to-pore distances close to 50 nm.

The creation of on-wafer microcavities for encapsulation further requires a special release-etching process to remove a sacrificial layer through the nanoporous membranes. Both silicon oxide and polymer sacrificial layers have been successfully etched through the nanoporous membranes using HF vapor and oxygen plasma, respectively. An extensive investigation of the HF vapor etching process resulted in identifying the process conditions needed for a successful release with no impact on the integrity of the nanoporous alumina membranes. Finally, the resulting microcavities have been sealed by depositing a metal (aluminum) or a dielectric (silicon nitride) film on the 200 mm wafers, thereby producing for the first time on-wafer micropackages of diverse shapes and configurations based on nanoporous alumina.

The exploration continued by integrating the new microencapsulation technology with Al-based interconnects (BEOL technology) to verify the compatibility of the new micropackages with standard IC and microsystems technology. Two different packaging configurations were successfully implemented on top of the metal interconnects. In one configuration, the PAA-based caps were sealed with 4 μm-thick SiN_z that is patterned to have the same lateral shape of the cap. In another packaging configuration, a 6 μm-thick SiN_z layer is used to seal the caps as well as cover the thin film interfaces at the cap edges (anchors) by laterally extending this sealing layer beyond the cap edges. This latter configuration was found to provide a significant improvement in the package resistance to air leakage. Moreover, encapsulated RF transmission lines were realized in order to study the RF characteristics of the new micropackages. Another result of this integration experiment is the realization of micropackages that have sufficient strength (with cap thicknesses up to 8.3 μm) to withstand the harsh process of plastic overmolding. A circular package of 0.22 mm diameter was found perfectly intact after an overmolding process performed at a pressure of 30 bar and a temperature of 175 °C. Furthermore, a package of similar dimensions (0.24 mm diameter) was also found intact—yet significantly deformed—after an overmolding process performed at a higher pressure of 90 bar. This investigation is an important achievement of this work as it bridges the gap

between wafer-level vacuum encapsulation of advanced microsystems and low-cost (plastic) packaging of traditional IC's.

Finally, another integration experiment has been launched to integrate the micropackages with Ni-based MEMS. This experiment facilitated the realization of microsensors (microresonators and Pirani gauges) aimed at pressure monitoring inside the micropackages, in addition to other microsystems like microswitches and micromirrors. The results of this integration process proved the basic compatibility of the micropackages with Ni-based microsystems. However, the use of a traditional sacrificial layer (silicon oxide) deposited at 400 °C caused noticeable damage to the Ni layer after completing the encapsulation process; thus limiting the usability (or yield) of the encapsulated MEMS.

6.1.2 Advanced design concepts

There is an apparent paradox in designing a "thin" package that is also strong and reliable in protecting the encapsulated device. However, achieving the right balance between miniaturization and strength is possible once the design constraints are clearly understood and analyzed by an accurate model. Therefore, a new model has been developed to describe the anisotropic behavior of the nanoporous alumina membranes. This model has subsequently been incorporated in different analytical models as well as finite element models that include all materials and geometry details of circular micropackages. The choice of a circular package shape is rather unconventional. However, it offers the advantages of perfect symmetry and the absence of sharp corners that are typically prone to stress and defect concentrations. Furthermore, basic flat plate deflection models suggest that a circular package experiences less stress and less deformation under hydrostatic loads, compared to a rectangular or square package of the same critical dimensions.

Using finite element models, an extensive study of the structural stability of the micropackages was performed. The impact of a number of factors has been investigated, including the package dimensions, use of a supporting pillar, residual stresses in the cap layers, temperature variations, and the ambient pressure. Important design guidelines have been drawn from this extensive study. As expected, a major factor in determining the package resistance to hydrostatic loads is its dimensions; namely the ratio of the lateral dimensions of the cap to its thickness. The higher this ratio the more sensitive the package becomes to hydrostatic loads. Moreover, the use of supporting pillars provides a significant reduction in the package deformation

under such hydrostatic loads although it does not lessen the stress introduced in the package. It is further observed that the structural stability of the micropackages can be improved by introducing a moderate compressive stress (around 100 MPa) into the upper (sealing) layer of the cap. This in combination with the slightly tensile stress in the nanoporous membranes results in a dome-shaped cap. Such dome shape is known to be more resistant to the impact of hydrostatic loads and is further shown (by simulations) to enhance the package endurance under extreme temperature variations.

Another area of advancement in package design is related to the encapsulation of RF microsystems. An enhanced design for a coplanar waveguide (CPW) compatible with the new micropackages has been established based on a simple and effective technique. The design concept is to locally narrow the buried RF feedthrough underneath the metal anchor of the package to reduce the undesired coupling between the CPW and the package anchor. This principle has been validated by 3D FEM simulations as well as by measurements of partially encapsulated CPW's. The measured RF performance of an encapsulated CPW with the improved feedthrough design is comparable to the performance of a typical CPW without encapsulation. However, if this narrowing of the buried feedthrough is not implemented, the encapsulated CPW exhibits a rather degraded RF performance—proving the effectiveness of the new design.

6.1.3 Proven good performance by measurements

"Meten is weten." This Dutch expression—which can be translated as "measurement is knowledge"—illustrates in a few rhythmic words how essential it is to extensively characterize any new engineered system in real life before judging on its performance. Therefore, significant efforts have been exerted in this work to characterize diverse aspects of the new micropackages. For example, this thesis reports the first long term hermeticity assessment (lasting more than 14 months) for different thin film packaging configurations based on nanoporous alumina. This extensive hermeticity test is based on optical detection of the deformation of thin caps during (or after) exposure to helium (at a high pressure of 3 bar) and air (at 1 bar). The results of this assessment show a clear difference in the obtained leak rate between He and air; with He leak rate being typically more than 2 orders of magnitude higher for the same package. This suggests a strong dependence of the hermeticity performance on the properties (or size) of the surrounding gas molecules. The test results further demonstrate the large impact of the package anchor configuration on hermeticity. It has been shown that

increasing the thickness of the silicon nitride sealing layer and extending it laterally beyond the edge of the Al anchor can result in nearly 40 times lower air leak rate. Moreover, very low air leak rates (less than 5×10^{-16} mbar.l/s) have been measured for the most hermetic micropackages (with the Al and silicon nitride cap layers extending across the whole chip). Such low leak rate corresponds to an internal pressure change of less than 150 mbar over a lifetime of 10 years under atmospheric pressure for a micropackage with a typical internal volume of 1 nl. One of the requirements of the hermeticity testing method based on optical detection of the cap deformation is the need for a reflective cap surface. Therefore, a Ti layer of 30 nm thickness is deposited on all samples measured with this technique. Although the presence of this Ti layer should not have a significant influence on the relative performance of the different package configurations, its absolute impact on the hermeticity of the micropackages is not well known. For more precise monitoring of the internal pressure of the micropackages, it has further been shown that miniature (embedded) Ni-based resonators and Pirani gauges can be used to monitor changes in pressure within the range of 0.1 to 100 mbar.

Another important realization of this work is assessing the reliability of the new PAA-based micropackages under extreme operational and storage conditions. Four different reliability tests have been used to evaluate the resistance of tens of micropackages to extreme thermomechanical and environmental stresses. The applied loads included mechanical shock (up to 200 g), temperature cycling (between –40 °C and +150 °C) as well as exposure to a combination of extreme heat and humidity levels (85% RH at 85 °C and 100% RH at 121 °C). By means of an optical gross leak test, it has been shown that most of the micropackages can withstand such extreme conditions without experiencing significant damage. Minor physical damage (partial delamination of a thin Ti layer) was only observed on 5 out of 16 micropackages submitted to the rather harsh pressure cooker test (100% RH at 121 °C, equivalent to a vapor pressure of 2 bar). No such damage was observed for the other three reliability tests: mechanical shock, temperature cycling, and high humidity exposure (85% RH at 85 °C).

6.2 Future challenges and opportunities

6.2.1 Materials and technology

A number of materials and processing techniques believed to be of high potential have been chosen as the focus of this research in order to maintain the scope and the required resources within feasible limits. First of all, the

basic choice of nanoporous alumina as an intermediate encapsulation layer has been motivated by the potentially simple production method and the unique properties of this material. However, a range of other porous materials that can serve the same purpose have been reported in recent literature (as in Table 1.2), each having its own features that can distinct it in certain applications. Furthermore, the main sacrificial and sealing layers used in this work are silicon oxide and silicon nitride, respectively. Preliminary demonstrations have also been shown using a polymer (photoresist) sacrificial layer as well as a metal (Al) sealing layer. Polymers in general are thermally and mechanically less stable than silicon oxide, although they can significantly reduce the thermal budget of the encapsulation process. Concerning Al (metal sealing), it is expected to be a more hermetic alternative to silicon nitride, although it is more prone to corrosion and it is considered less compatible with RF microsystems that require non-reflecting (dielectric) surroundings.

In terms of process technology, this work presents a simple and cost-effective Al anodization process for the production of nanoporous alumina membranes. However, other processes involved in the encapsulation sequence are still considered as more costly (time consuming). For example, the vapor HF etching process for the sacrificial silicon oxide layer removal lasts for 30–40 minutes per micrometer of sacrificial oxide thickness. Moreover, there are no manufacturing tools available at the moment that can perform this HF vapor etching process simultaneously on a large number of wafers. To overcome the relatively high cost of this etching process, work is needed to improve the process stability and speed.

Another challenge perceived in this work is the compatibility of the encapsulation process (using an oxide sacrificial layer deposited at 400 °C) with Ni-based microsystems. Some effort is still needed to either mitigate the impact of high-temperature processing on the Ni microstructures or lower the thermal budget of the encapsulation process. Mitigating the impact of high temperature exposure can be achieved by altering the crystallographic properties of the Ni layer by optimizing the deposition process or by alloying the Ni with other elements (Golodnitsky *et al.*, 2002; Kelly *et al.*, 2003). Alternatively, lowering the thermal budget of the encapsulation process can be realized by using a different sacrificial material (*e.g.*, a polymer) or a different deposition process for the sacrificial oxide layer. Finally, the compatibility of the encapsulation process with other MEMS or microsystems materials and technologies is another interesting area for future research.

6.2.2 Micropackage design and performance

It has been shown in this work that understanding the thermomechanical characteristics of new microstructures is crucial to maturing them into functional and reliable devices. In particular, the residual stresses and stress variations in thin films are a major source of instability in surface micromachined structures. Besides the impact of the deposition process on thin film stresses; the thermal mismatch, geometrical details and boundary conditions of the entire microstructure would play an important role in the final stress configuration. Hence, future challenges in thermomechanical modeling and design are foreseen when new materials, processes or geometrical designs are introduced.

Concerning the performance and functionality of the micropackages, future work should focus on the area of hermeticity improvement and testing. Monitoring the internal pressure of the micropackages (using an embedded microsensor) can be helpful for further hermeticity analysis. If required, a lower internal package pressure and better stability over time can be achieved by further optimizing the sealing process or by incorporating thin film getters. Moreover, studying the outgassing properties of the internal surfaces of the micropackages can further provide more insight into the composition and evolution of the internal environment of the microcavities. It is also important to consider the exact pressure and hermeticity requirements of the final application of the micropackages (these requirements can largely vary depending on the application).

6.2.3 New applications for nanoporous alumina

As demonstrated in this work, micropackages based on nanoporous alumina can provide reliable protection and connectivity for microsystems featuring mechanical, electrical or RF functionalities. Nevertheless, the full potential of nanoporous alumina in the field of microsystems (packaging) is yet to be reached. For example, caps composed of nanoporous alumina and PECVD silicon nitride—which are both fairly transparent to visible light—can be used to encapsulate optical microsystems (or MOEMS) as illustrated in Fig. 6.1(a). Furthermore, pressure or force sensors can be constructed based on metal-sealed microcavities with a stable internal pressure. The concept of such sensor is shown in Fig. 6.1(b). Cap deformations due to an external pressure or force can be translated by this device into an electric signal triggered by the capacitance change between the cap and an internal electrode.

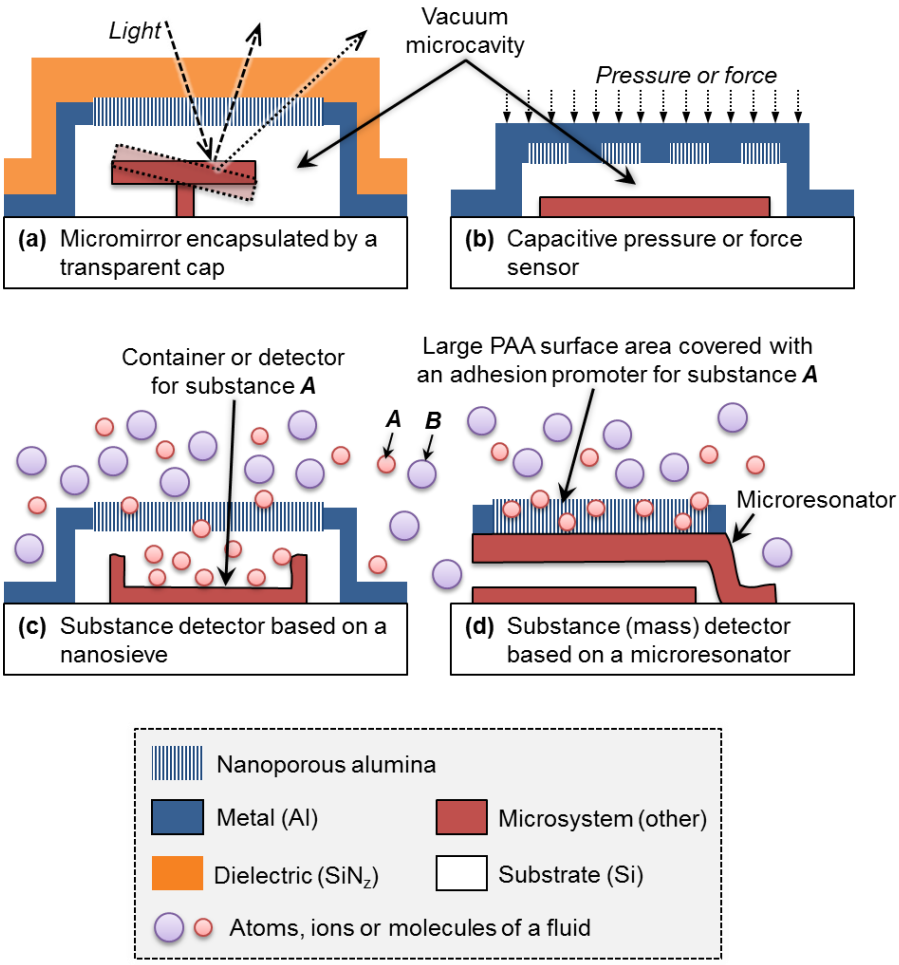


Fig. 6.1 Conceptual schematics of four different microsystems that can be realized by using thin membranes of nanoporous alumina (PAA): (a) a micromirror encapsulated by a thin transparent cap; (b) a pressure or force sensor based on a sealed cavity and two metal electrodes; (c) a detector of a specific gas or fluid (with a nanosieve based on PAA); and (d) mass detector based on a PAA membrane attached to a microresonator. Here it is assumed that the atoms (or ions or molecules) of substance ***A*** are effectively smaller than the pores of the PAA membranes.

Not only electromechanical, RF and optical microsystems, but also the areas of microfluidics and environmental sensors can benefit from the new nanoporous alumina membranes. As mentioned in Chapter 1, porous alumina

membranes with any pore diameter between 2 and 900 nm can be produced by a simple Al anodization process. Hence, one can easily produce nanosieves (Tong *et al*., 2004) at wafer-level using nanoporous alumina membranes. Such nanosieves can then be used in different applications such as on-chip fluid separation or detection as conceptually illustrated in Fig. 6.1(c).

Another distinct feature of nanoporous alumina membranes is their exceptionally large surface area to volume ratio. This feature can be exploited for example in environmental sensing applications where the large surface area can act as a collector (*e.g.*, by using an adhesion promoter) for particular atoms or molecules. The collected matter (or added mass) at the surface of the nanoporous membranes can be detected for example through a change in the resonance properties of a microresonator (Waggoner and Craighead, 2007) as schematically shown in Fig. 6.1(d). The collected matter can alternatively be detected by means of monitoring a different physical property (like the dielectric constant) of the nanoporous membranes.

The above is only an attempt to illustrate the possibilities associated with integrating nanoporous alumina with modern microsystems. Looking from a wider perspective, one may think of countless other potential applications of nanoporous alumina. Areas like energy storage (or generation), nanofabrication and even quantum computing can also benefit from the unique structure of the long and narrow nanopores of this material (which can be easily produced at a large scale). If time and space are plentiful, one's limit in listing and describing such possibilities and applications would only be one's own imagination!

"Discovery consists of seeing what everybody has seen and thinking what nobody has thought."

Albert Szent-Györgyi (1893–1986)

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"A thinker sees his own actions as experiments and questions—as attempts to find out something. Success and failure are for him answers above all."

Friedrich Wilhelm Nietzsche (1844–1900)

Curriculum vitae

Joseph Eid Estafanous Zekry was born in Aswan, Egypt, in January 1984. In July 2000, he was named in the national honors list for the best secondary school graduates in Egypt. In June 2005, he received the B.Sc. degree in Electrical Engineering with *distinction and honor* from Ain Shams University in Cairo, Egypt. Between September 2005 and August 2007 he was awarded several scholarships for teaching and research activities in physics, microelectronics and MEMS from the American University in Cairo, Egypt, as well as KU Leuven and imec in Leuven, Belgium. In June 2007, Mr. Zekry was awarded the M.Sc. degree in physics from the American University in Cairo, Egypt. His M.Sc. research dealt with thin film technology and the design of high force MEMS switches. From August 2007 until May 2008, he received a research fellowship to work in the field of solid state devices at Rensselaer Polytechnic Institute in Troy, NY, USA. Between August 2008 and December 2012 he conducted the research presented in this dissertation at KU Leuven and imec in Leuven, Belgium, where he developed new MEMS and thin film encapsulation technologies at the 200 mm fabrication facilities in imec. Between 2008 and 2012, he was also a member of the consortium of MEMSPACK—a collaborative research project funded by the European Commission for the development and characterization of generic 0- and 1-level packaging technologies for RF-MEMS. Since February 2013, he has been working on the development of new wafer topography measurement systems for advanced photolithography machines at ASML in Veldhoven, The Netherlands.

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